



A890GXM-A

VER : 1.0

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REVISION HISTORY:

Rev	Date	Notes
A	20091105	First release.
B	20091228	Page 11:Add ER11.(for CPU NB power fail),BOM R174 del(for no CPU power). Page 17:NB pin A8 & B8 change pin name,pin D10 del(for DP can't display). Page 19:Add PCI-E and DP switch pin(for PCI-E and DP switch). Page 21:Add C175,C176 and change MN3 pin S to TMDS_HPD0(for DP can't display). Page 22:Add cap and change circuit(for VGA noise). Page 23:Add X6,R310,C277,C278(for can't power on). Page 24:Change IMC_TDI,IMC_TDO,IMC_TRST_ pin and add GBE LAN PHY not used pull H/L. Page 26:Add GBE LAN PHY not used connect to GND. Page 34:R277、R278 change to RJ14、RJ15 and change power source(for EuP function).

1.0

20100115

Page 21:Add R314.(for 插入D-SUB,DVI & HDMI cable造成漏電，讓DP HPD_D有約0.3V造成誤動作).

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

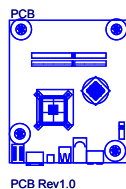
1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.



PCB Rev1.0

PCB Impedance control

Impedance (OHM)	Trace Width (mil)	(S/W/S)	Trace Length (inch)	Pre-preg	Default
50	4	(20/4/20)	8	1080	V

1)Circuit type 1

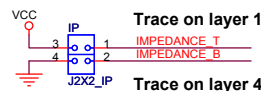
Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM

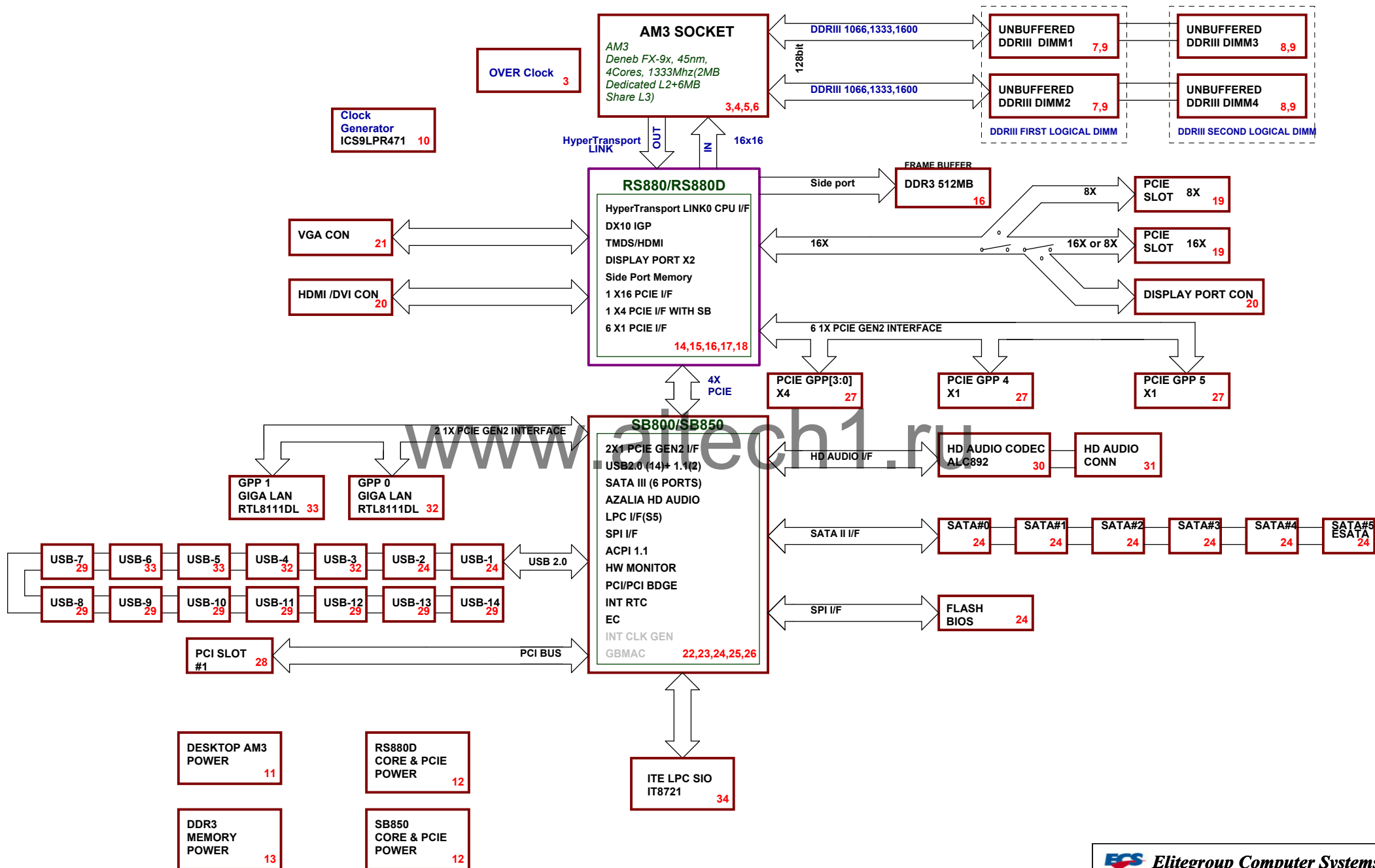
PCB STACK:



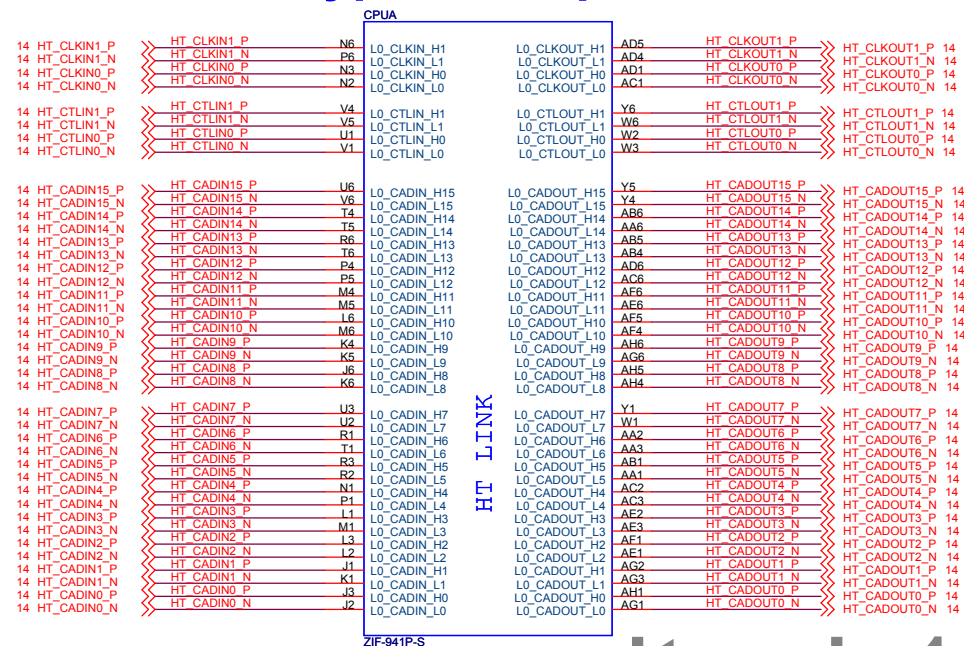
PCB P/N:15-R57-011000

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

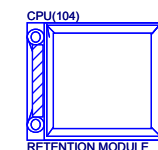
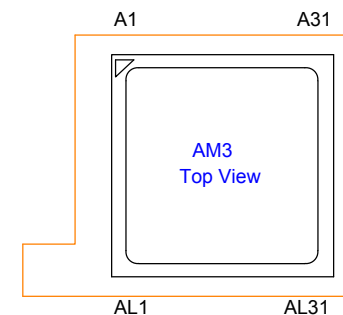
ECS Elitegroup Computer Systems	
Title	
COVER PAGE	
Size	Document Number
Custom	A890GXM-A
Date:	Monday, January 18, 2010
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HyperTransport

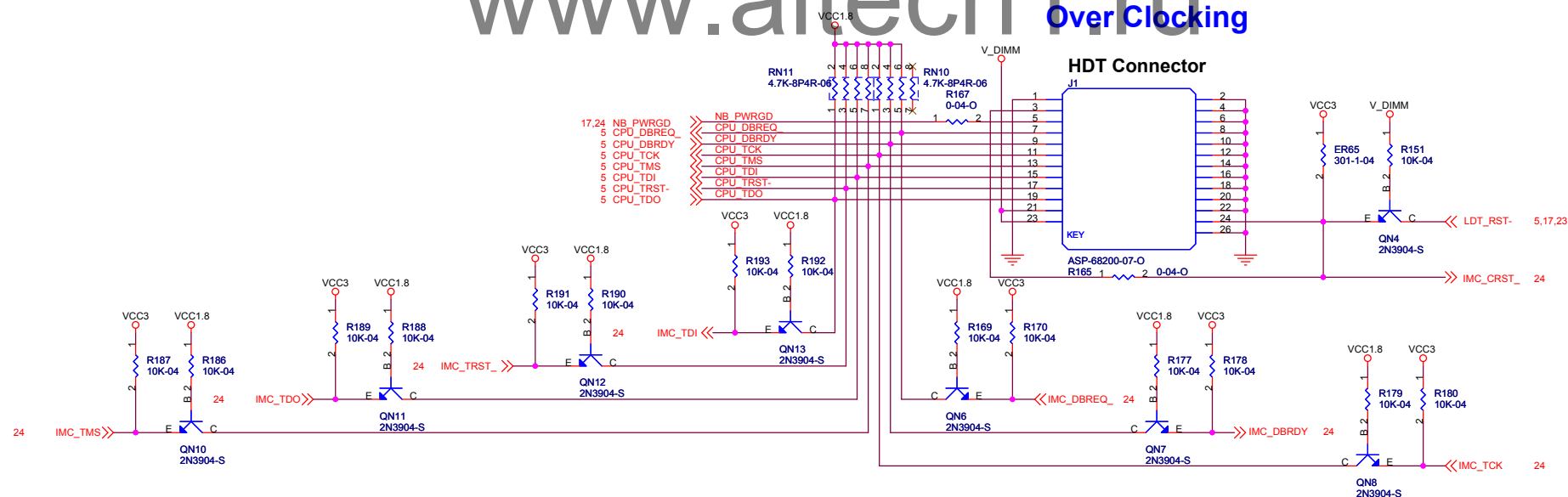


Please use 1mm pad size,
place all ELT test pads
on bottom side only.



The image shows a close-up of a circuit board with a large, semi-transparent watermark 'www.aitech1.ru' overlaid. A red dot is marked on the board, labeled 'VCC1.8'. In the top left corner, there is a small blue box containing the text 'ZIF-941P-S'. In the bottom right corner, the text 'Over Clock' is visible in blue.

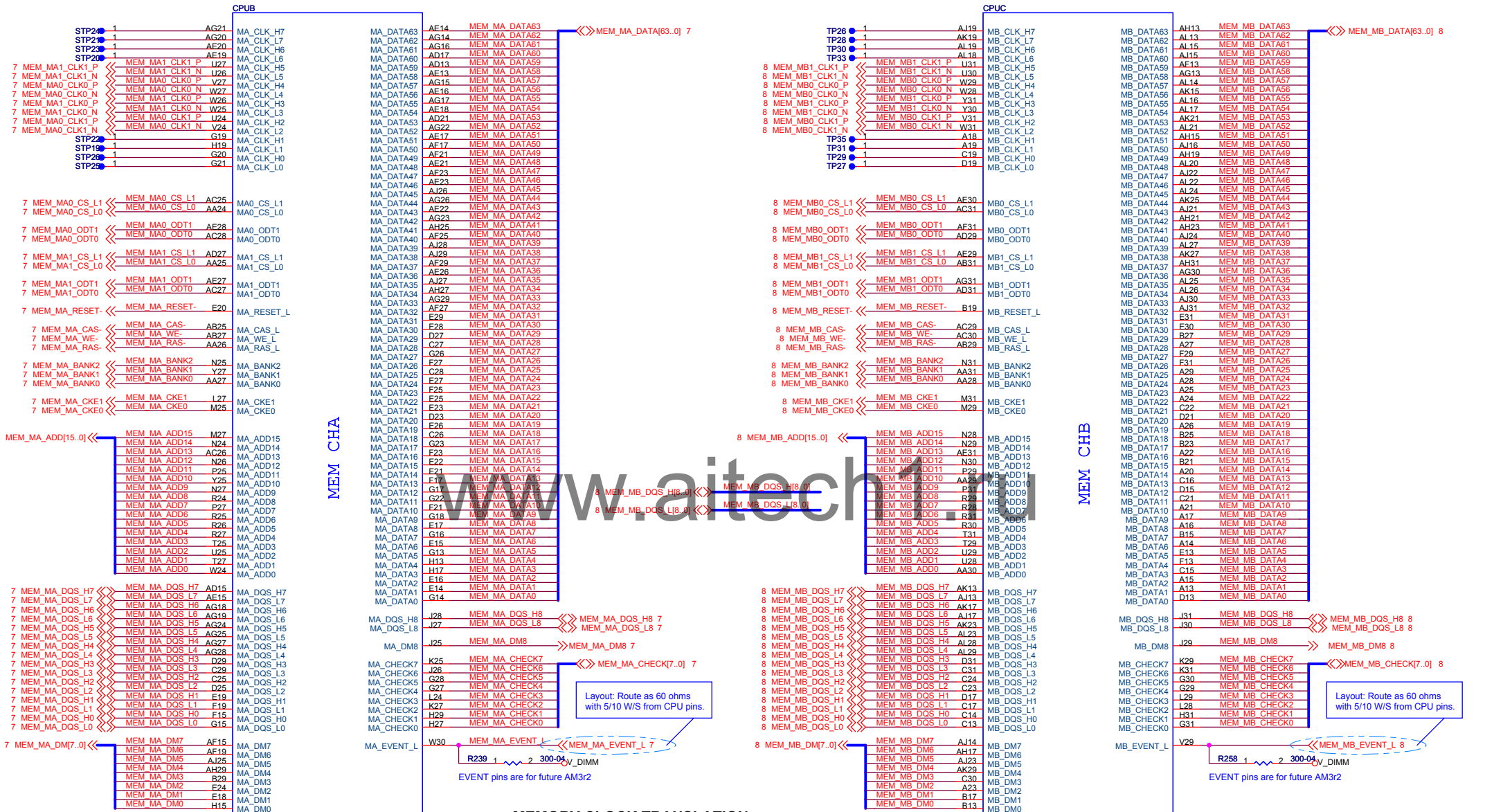
Over Clocking



DDR3 Memory Interface A

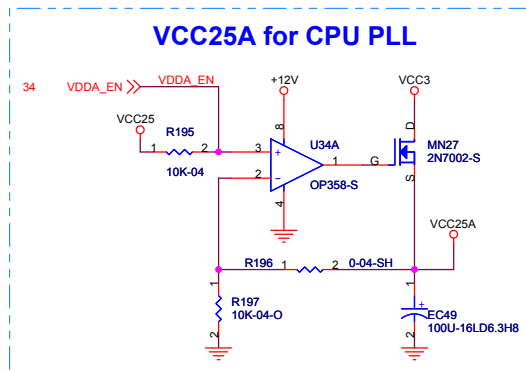
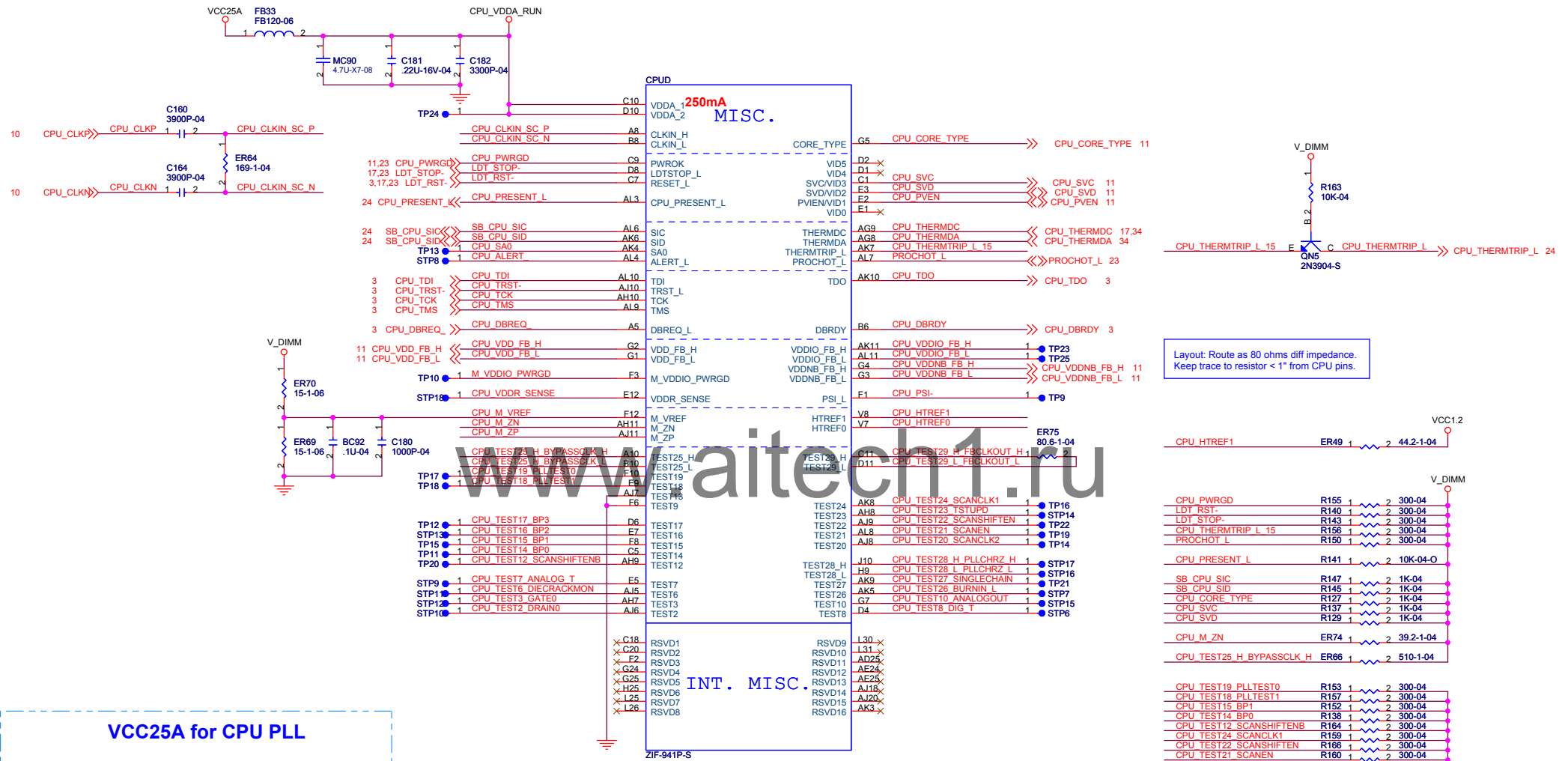
CPU Memory

DDR3 Memory Interface B

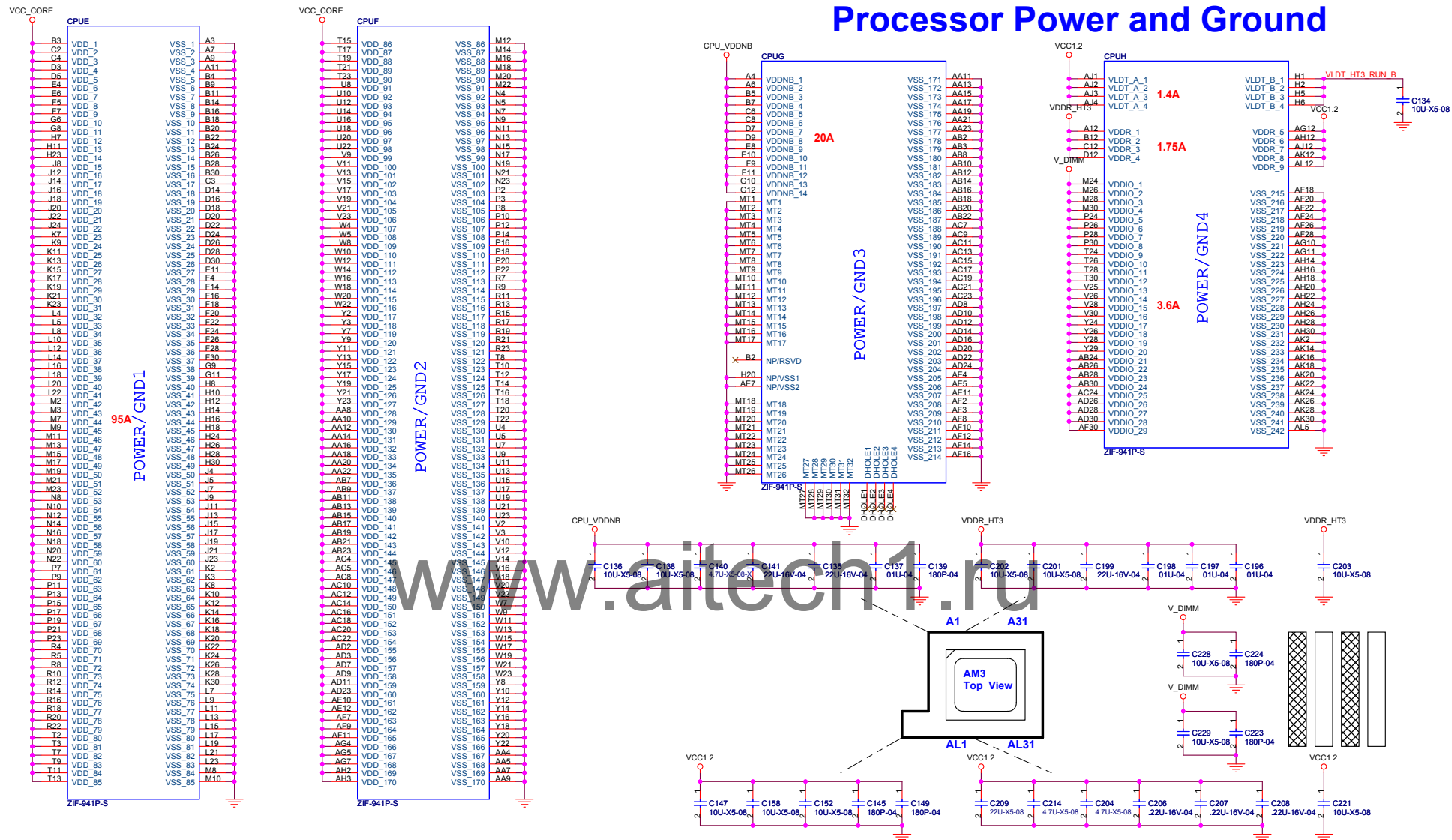


MEMORY CLOCK TRANSLATION

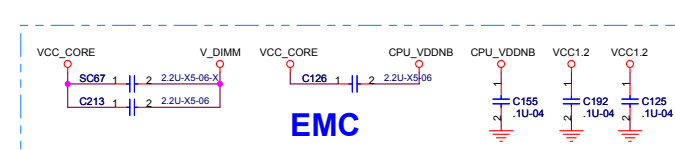
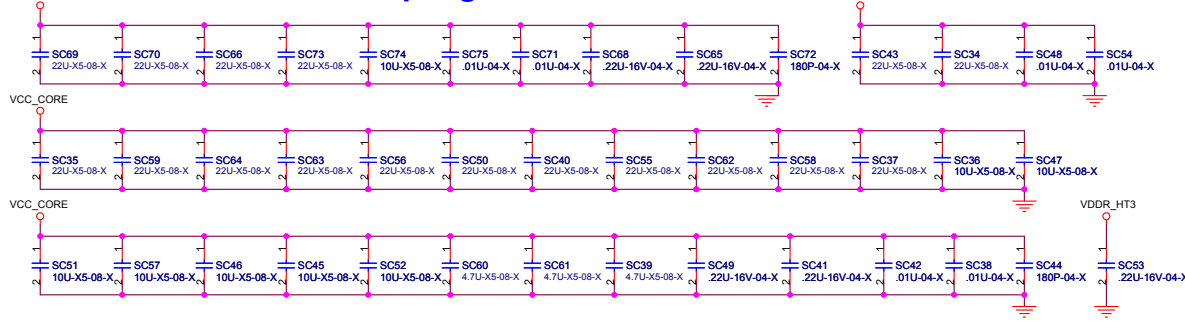
DIMM	DDR2 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK1	MA_CLK2
	MEM_MA0_CLK0	MA_CLK4
DIMM A1	MEM_MA1_CLK1	MA_CLK5
	MEM_MA1_CLK0	MA_CLK3
DIMM B0	MEM_MB0_CLK1	MB_CLK2
	MEM_MB0_CLK0	MB_CLK4
DIMM B1	MEM_MB1_CLK1	MB_CLK5
	MEM_MB1_CLK0	MB_CLK3



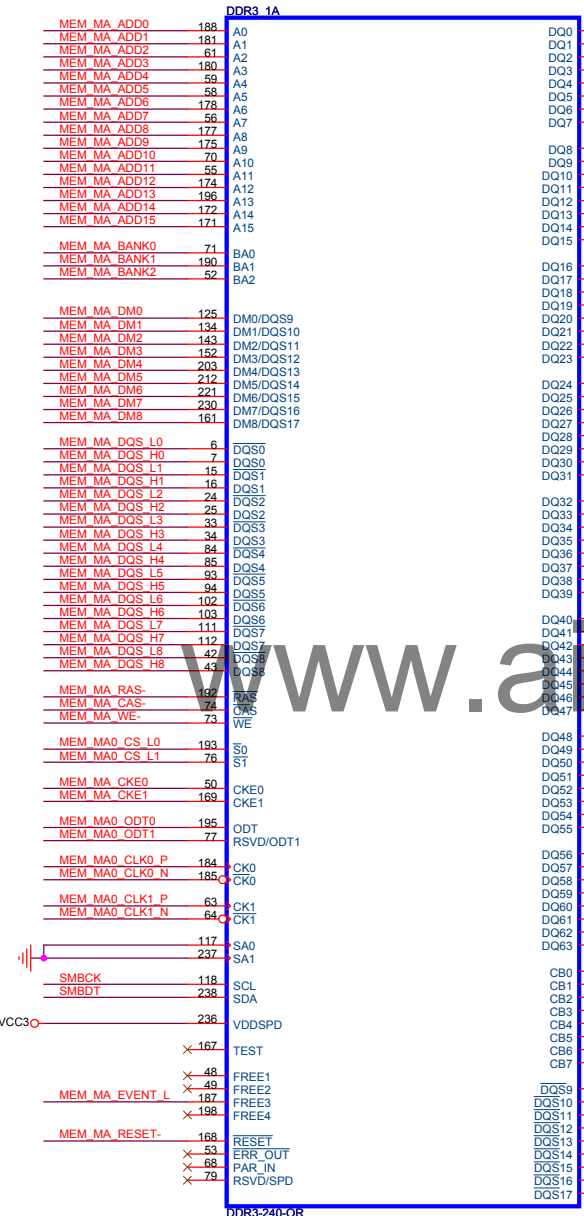
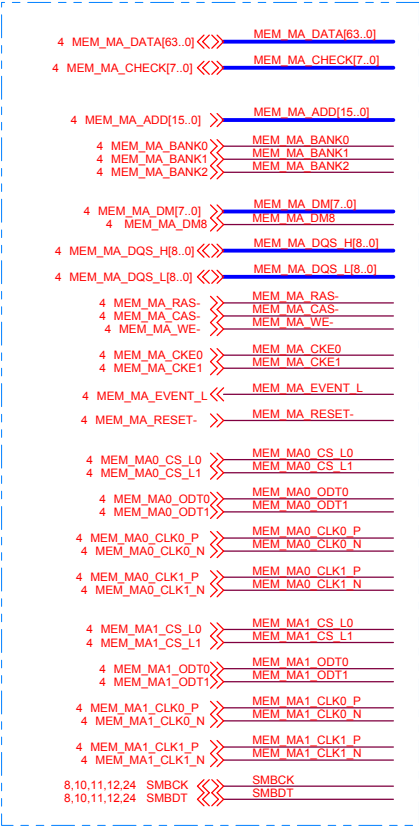
Processor Power and Ground



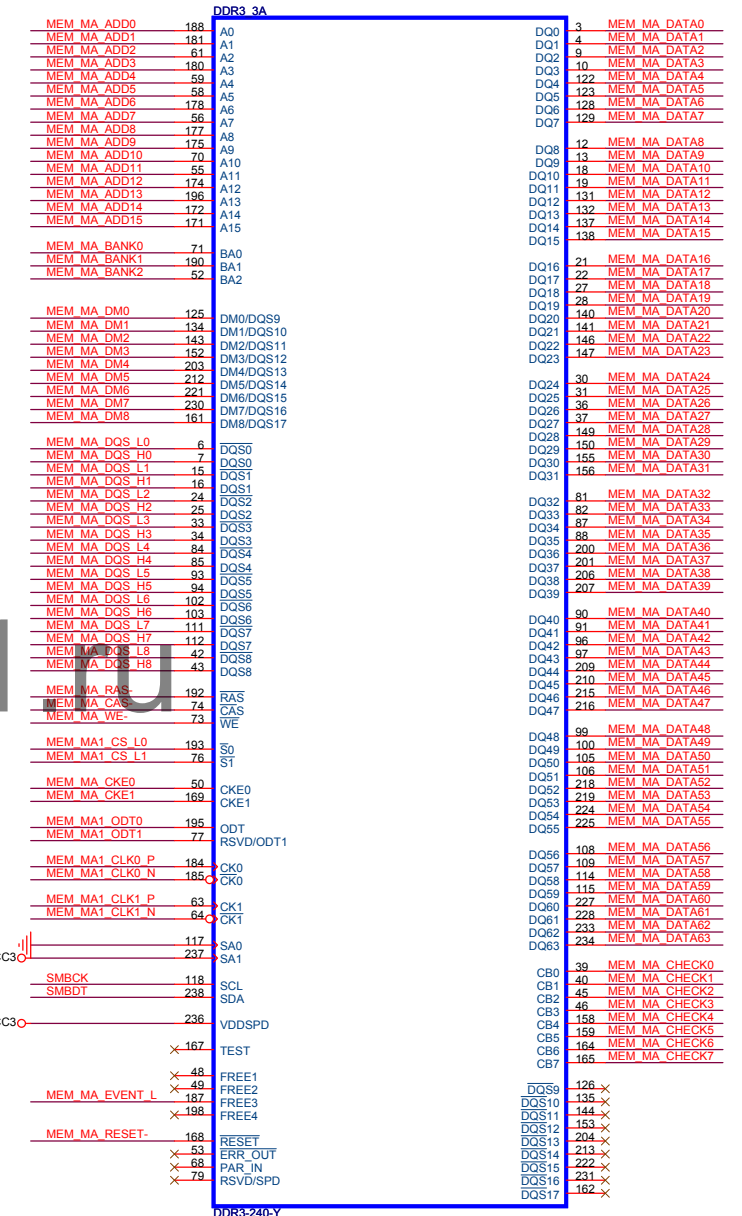
Bottom Side Decoupling



External Connection



A Chanel



SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

External Connection

4 MEM_MB_DATA[63..0] <<<>	MEM_MB_DATA[63..0]
4 MEM_MB_CHECK[7..0] <<<>	MEM_MB_CHECK[7..0]
4 MEM_MB_ADD[15..0] <<<>	MEM_MB_ADD[15..0]
4 MEM_MB_BANK0 <<<>	MEM_MB_BANK0
4 MEM_MB_BANK1 <<<>	MEM_MB_BANK1
4 MEM_MB_BANK2 <<<>	MEM_MB_BANK2
4 MEM_MB_DM[7..0] <<<>	MEM_MB_DM[7..0]
4 MEM_MB_DM8 <<<>	MEM_MB_DM8
4 MEM_MB_DQS_H[8..0] <<<>	MEM_MB_DQS_H[8..0]
4 MEM_MB_DQS_L[8..0] <<<>	MEM_MB_DQS_L[8..0]
4 MEM_MB_RAS- <<<>	MEM_MB_RAS-
4 MEM_MB_CAS- <<<>	MEM_MB_CAS-
4 MEM_MB_WE- <<<>	MEM_MB_WE-
4 MEM_MB_CKE0 <<<>	MEM_MB_CKE0
4 MEM_MB_CKE1 <<<>	MEM_MB_CKE1
4 MEM_MB_EVENT_L <<<>	MEM_MB_EVENT_L
4 MEM_MB_RESET- <<<>	MEM_MB_RESET-
4 MEM_MB0_CS_L0 <<<>	MEM_MB0_CS_L0
4 MEM_MB0_CS_L1 <<<>	MEM_MB0_CS_L1
4 MEM_MB0_ODT0 <<<>	MEM_MB0_ODT0
4 MEM_MB0_ODT1 <<<>	MEM_MB0_ODT1
4 MEM_MB0_CLK0_P <<<>	MEM_MB0_CLK0_P
4 MEM_MB0_CLK0_N <<<>	MEM_MB0_CLK0_N
4 MEM_MB0_CLK1_P <<<>	MEM_MB0_CLK1_P
4 MEM_MB0_CLK1_N <<<>	MEM_MB0_CLK1_N
4 MEM_MB1_CS_L0 <<<>	MEM_MB1_CS_L0
4 MEM_MB1_CS_L1 <<<>	MEM_MB1_CS_L1
4 MEM_MB1_ODT0 <<<>	MEM_MB1_ODT0
4 MEM_MB1_ODT1 <<<>	MEM_MB1_ODT1
4 MEM_MB1_CLK0_P <<<>	MEM_MB1_CLK0_P
4 MEM_MB1_CLK0_N <<<>	MEM_MB1_CLK0_N
4 MEM_MB1_CLK1_P <<<>	MEM_MB1_CLK1_P
4 MEM_MB1_CLK1_N <<<>	MEM_MB1_CLK1_N
7,10,11,12,24 SMBCK <<<>	SMBCK
7,10,11,12,24 SMBDT <<<>	SMBDT

VCC3
237
SMBCK
SMBDT
238
VDDSPD
236
167
TEST
48
FREE1
49
FREE2
187
FREE3
190
FREE4
168
RESET
53
ERR_OUT
68
PAR_IN
79
RSVD/SPD

SA0
SA1
SCL
SDA

VDDSPD

TEST

FREE1

FREE2

FREE3

FREE4

RESET

ERR_OUT

PAR_IN

RSVD/SPD

167

48

49

187

190

168

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RSVD/SPD

167

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RSVD/SPD

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RSVD/SPD

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RSVD/SPD

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RSVD/SPD

167

48

49

187

190

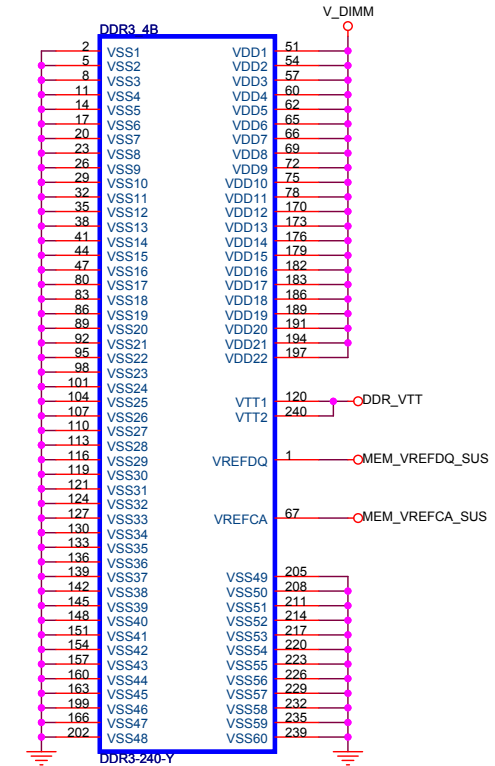
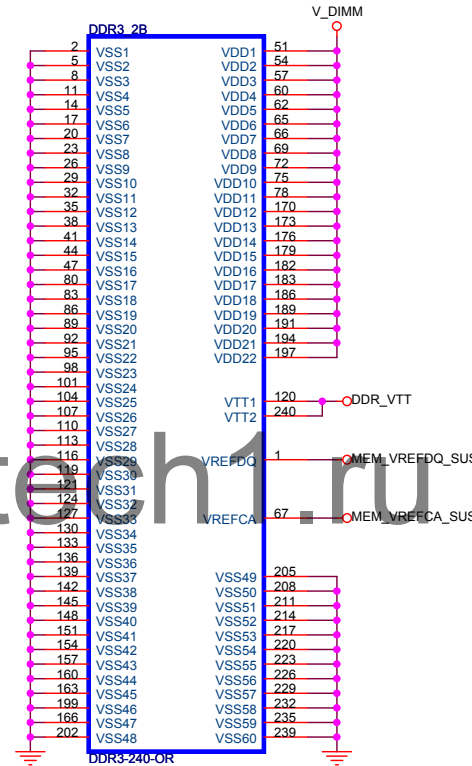
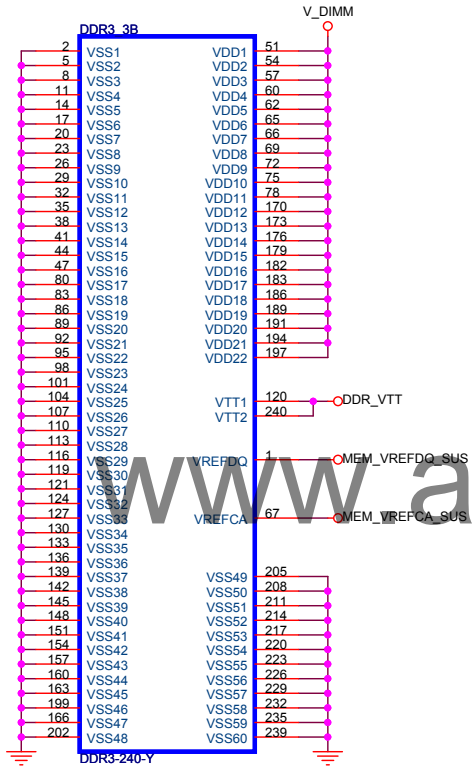
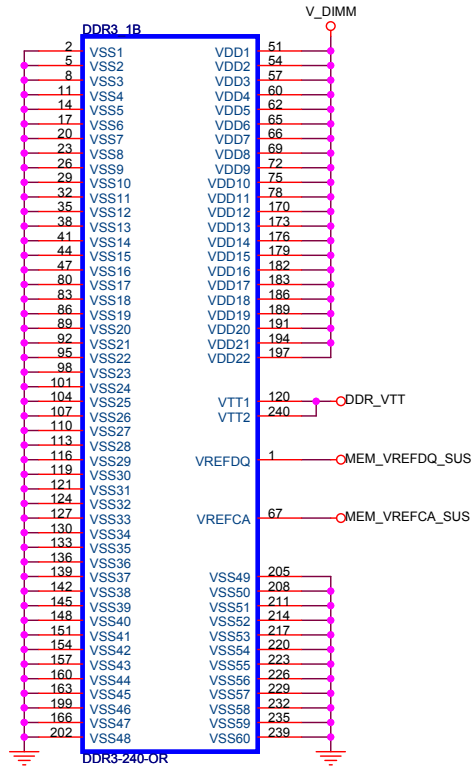
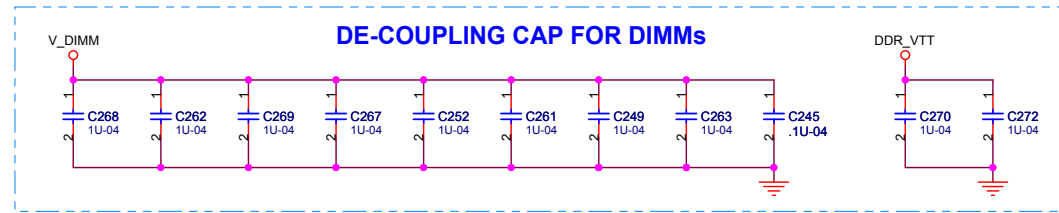
168

53

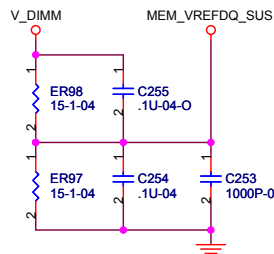
68

79

RSVD/SPD

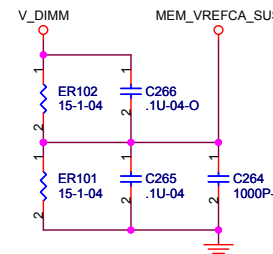


MEM_VREFDQ_SUS

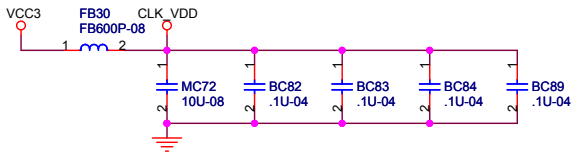


Layout: Place within 500 mils of the DIMM4 socket.

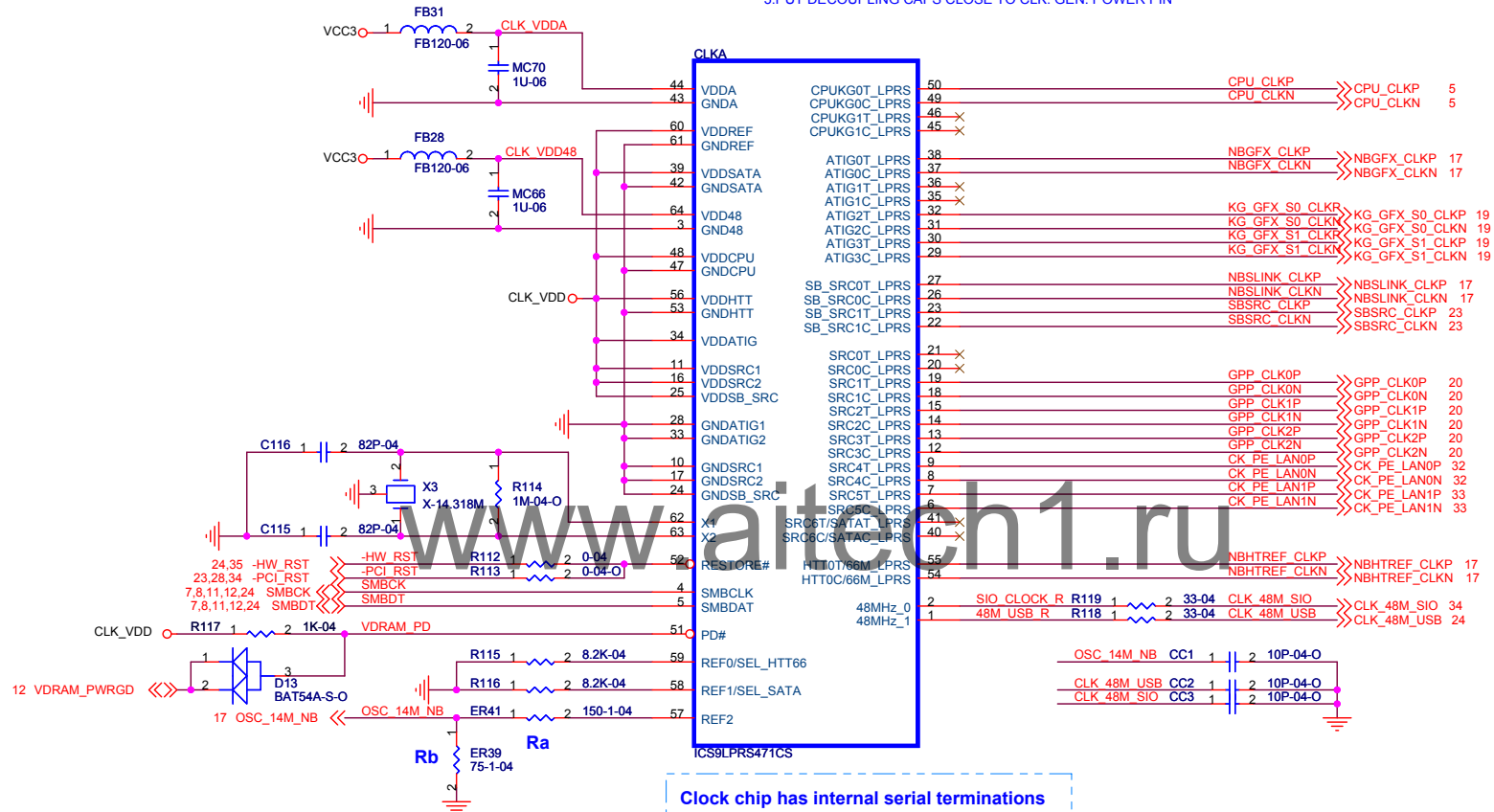
MEM_VREFCA_SUS



Layout: Place within 500 mils of the DIMM4 socket.



- 1.PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLK. GEN. AS POSSIBLE
- 2.ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3.PUT DECOUPLING CAPS CLOSE TO CLK. GEN. POWER PIN



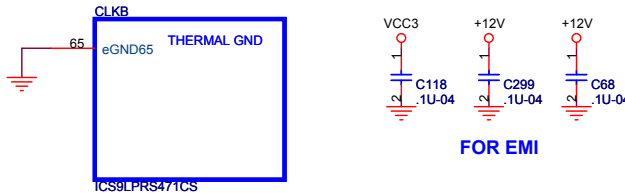
RS890 OSC_14M_NB 1.1V Ra/Rb=150R/75R

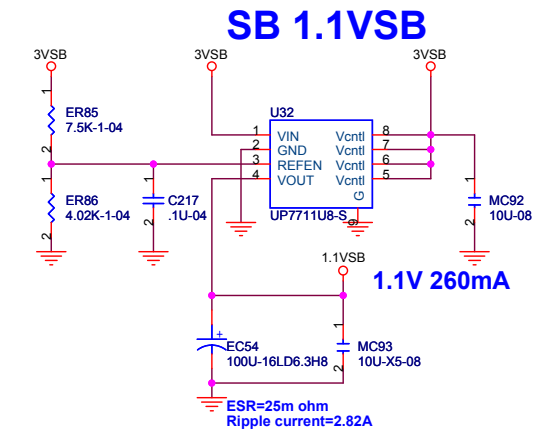
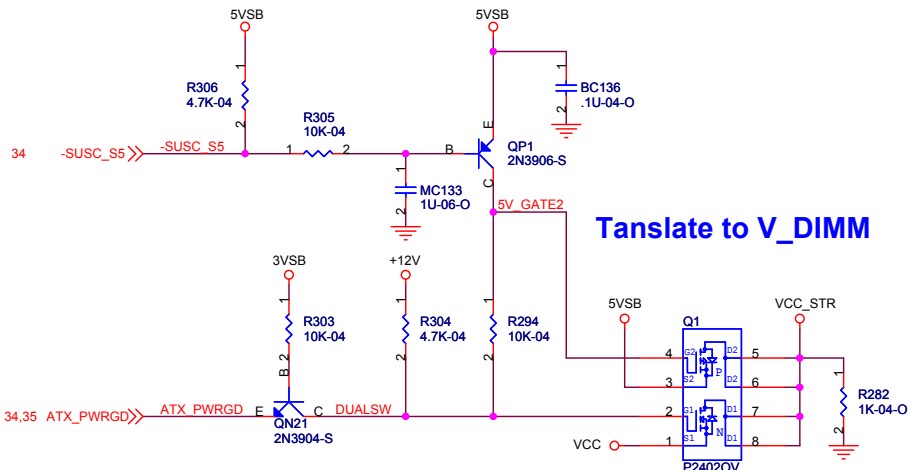
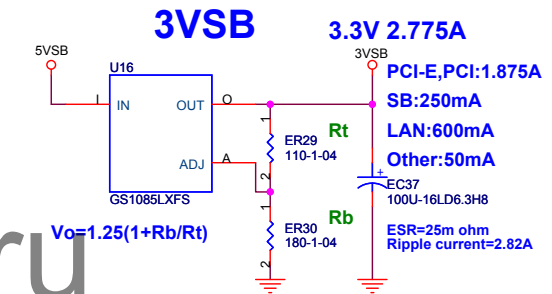
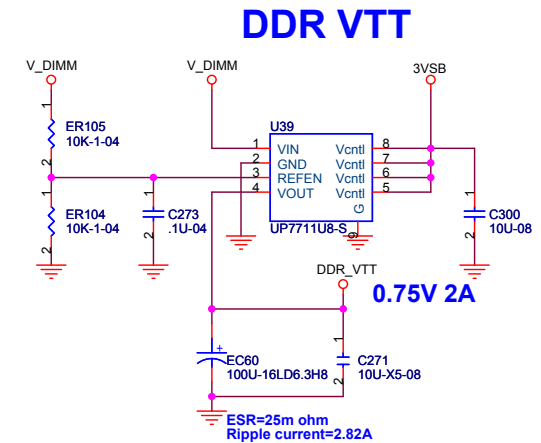
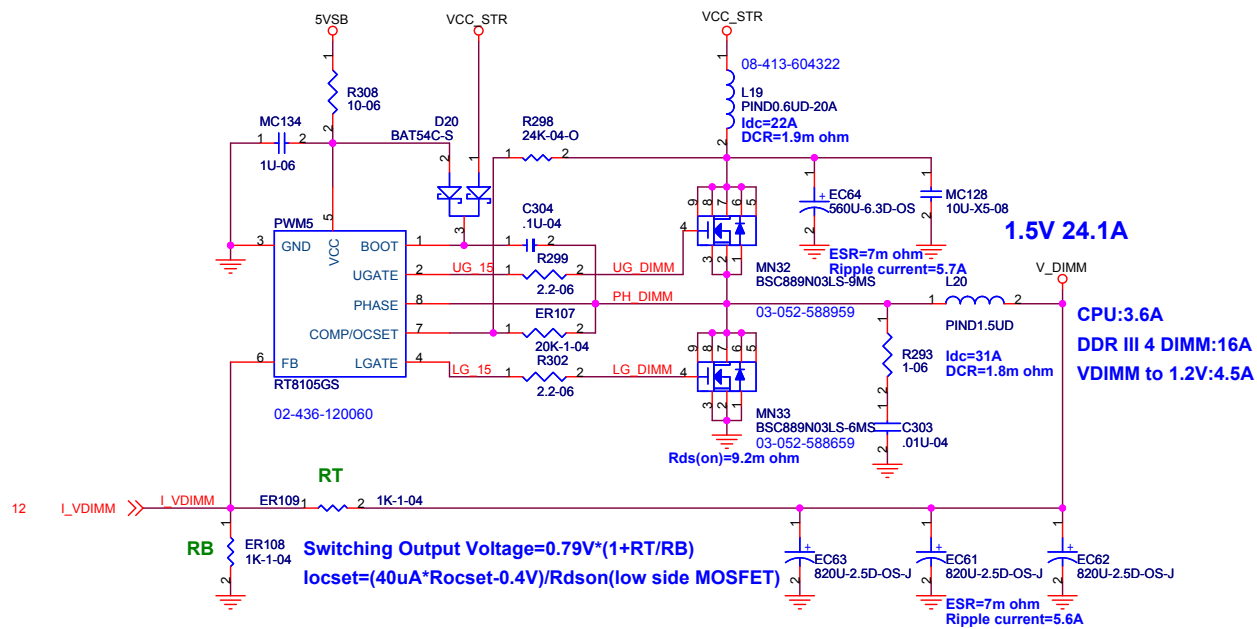
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

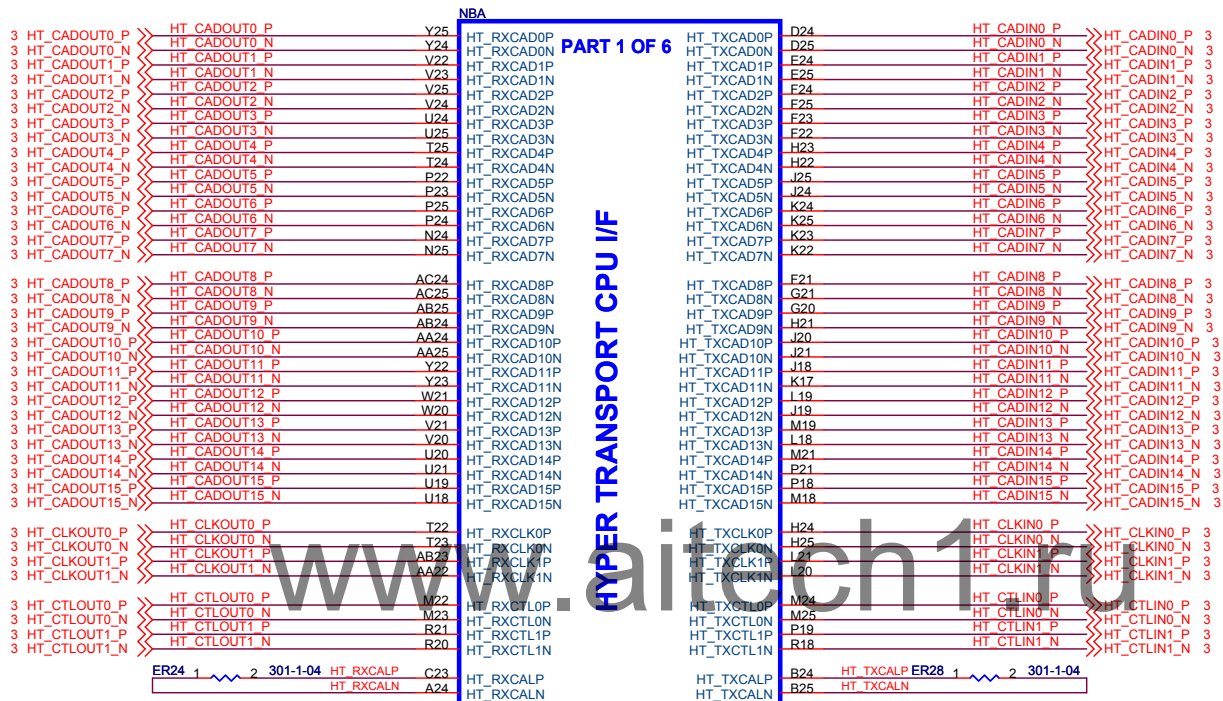
REF0/SEL_HTT66	HTT CLOCK
0 *	100 MHz differential HTT clock
1	66 MHz 3.3V single ended HTT clock

REF1/SEL_SATA	SRC6/SATA
0 *	100 MHz spreading differential SRC clock
1	100 MHz non-spreading differential SRC clock

* default



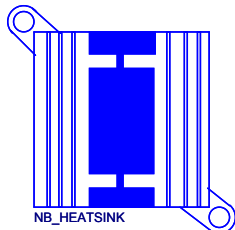




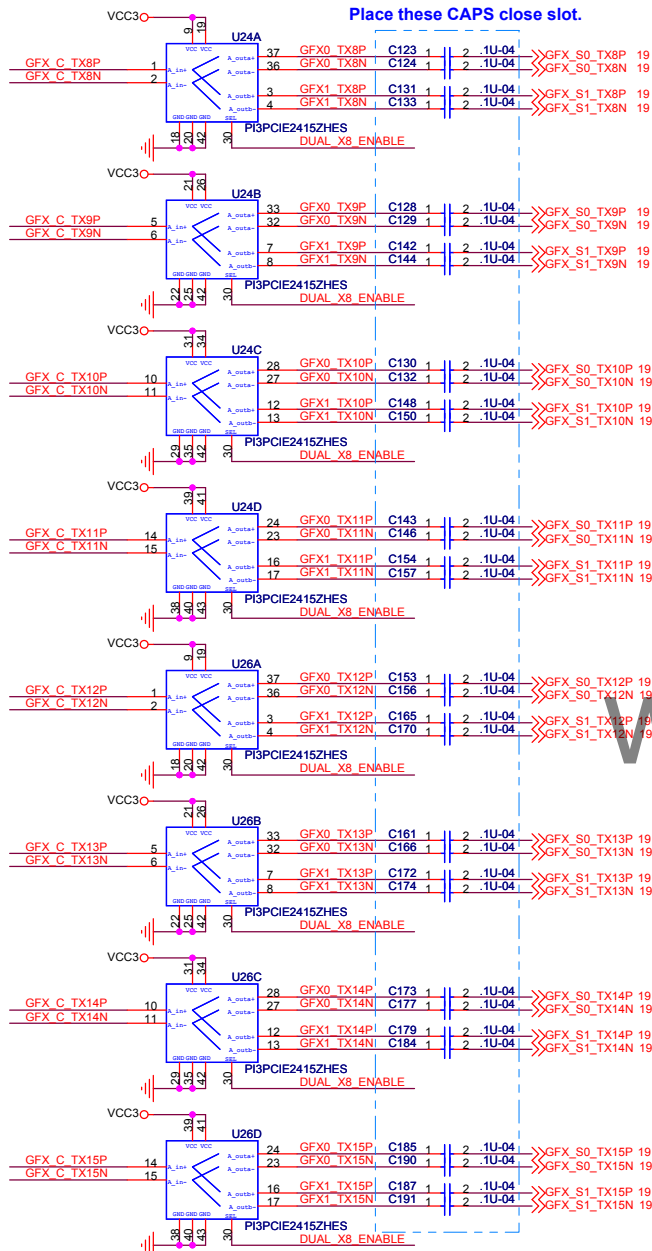
RS880D A11
 890GX
 01-201-880160

TDP:25W

NB(104)



ECS Elitegroup Computer Systems			
Title RS880D HT LINK I/F			
Size Custom	Document Number A890GXM-A		Rev 1.0
Date:	Thursday, January 14, 2010		Sheet 14 of 38



RS880D GFX Slot Routing table

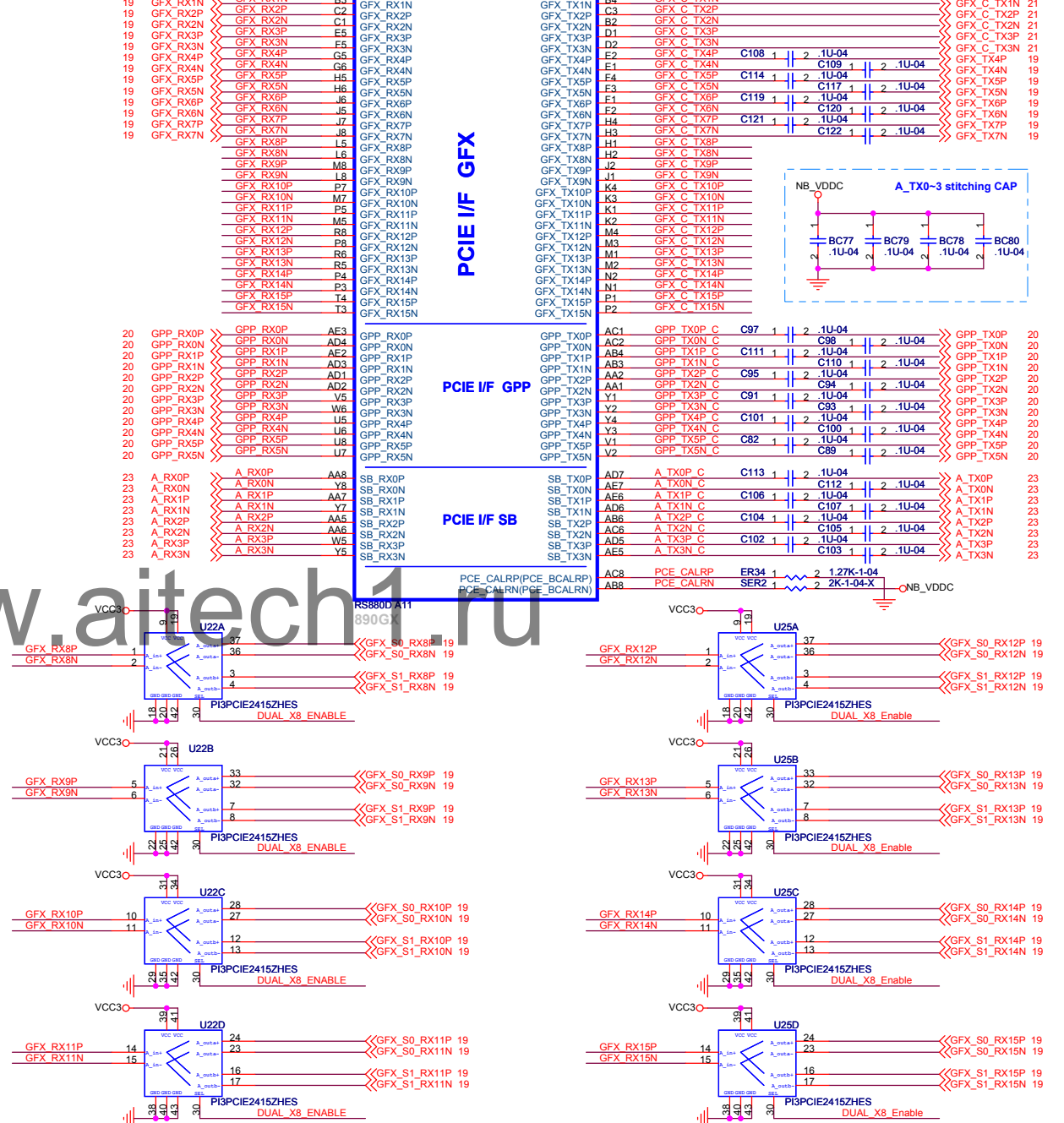
GFX_MODE_SELECT	GFX SLOTS MODE
0	X16 LANES MODE (DEFAULT)
1	TWO X8 LANES MODE

RS880D GPP Routing table

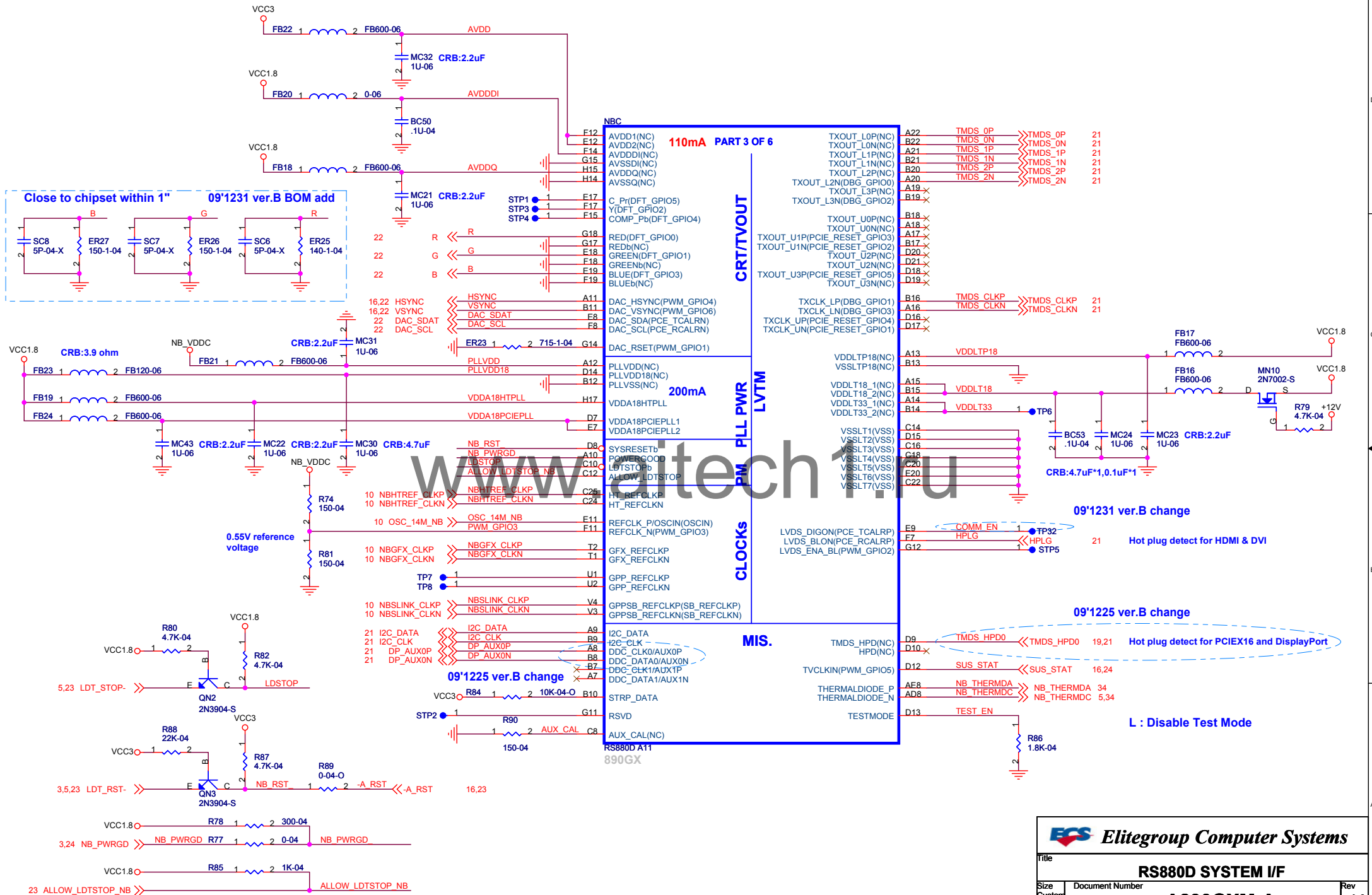
RS880D GPP LINE	
GPP[3:0]	PCIE X4 SLOT
GPP4,5	PCIE X1 SLOT * 2

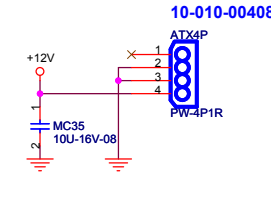
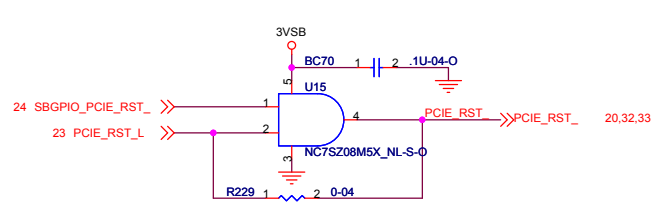
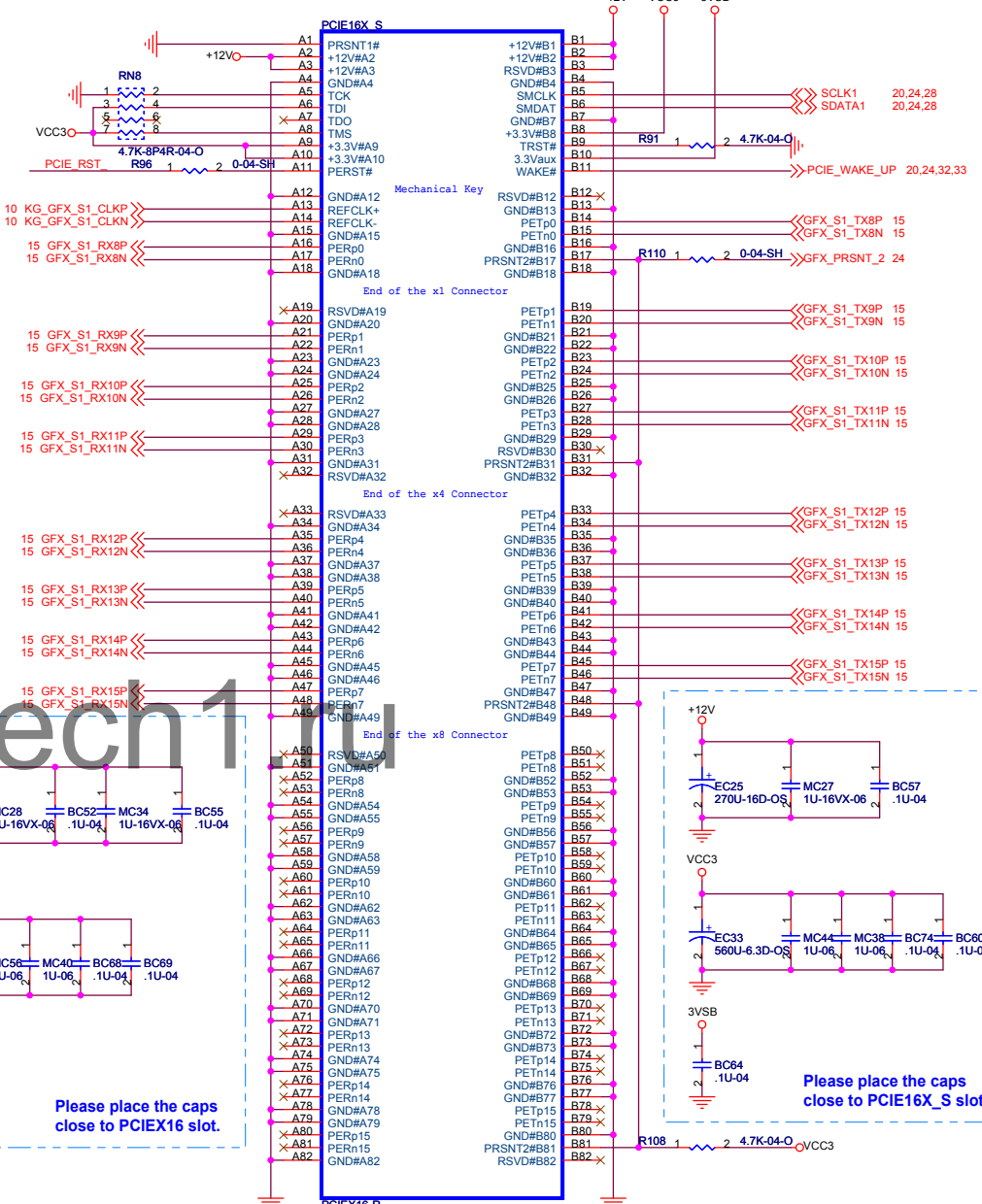
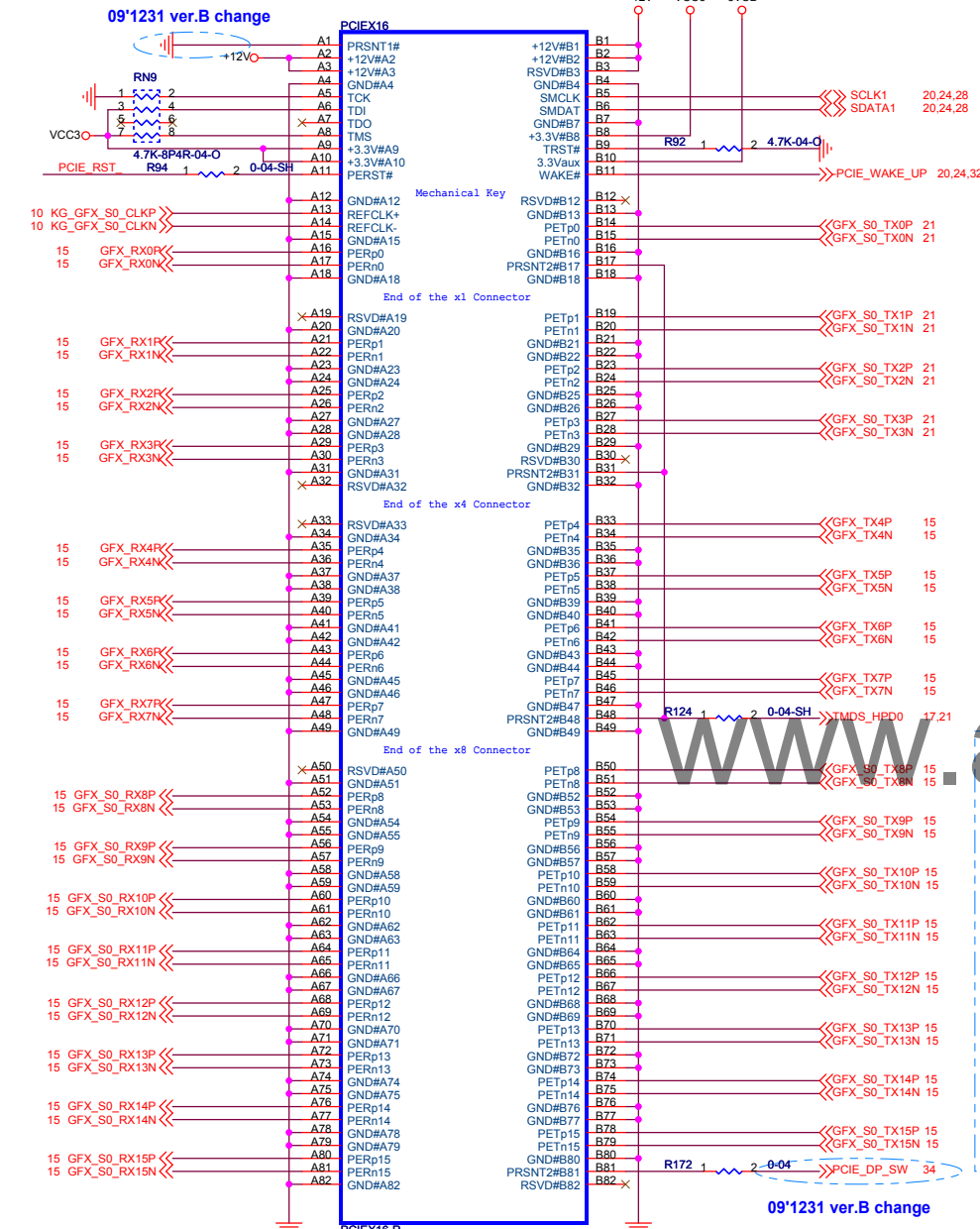
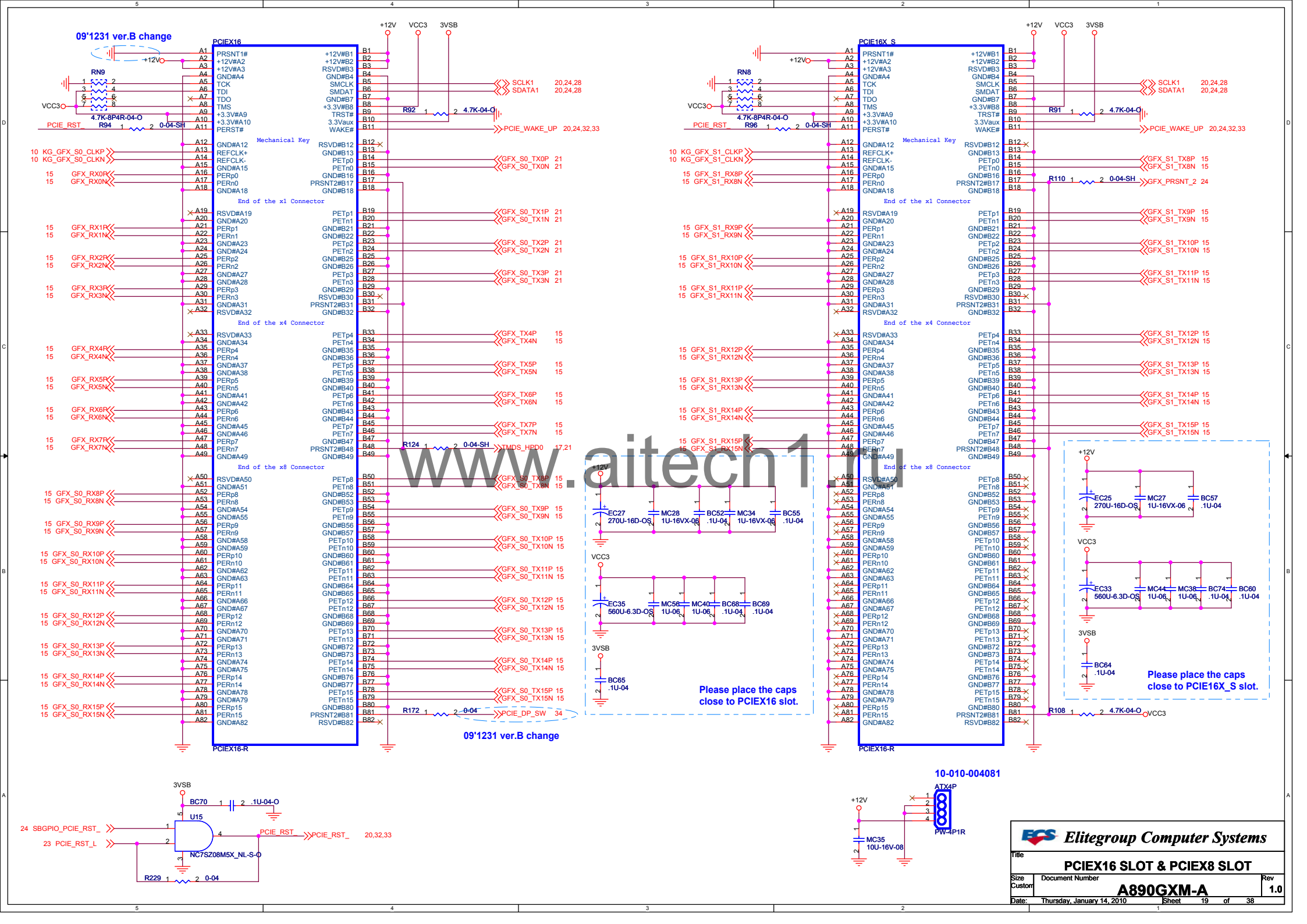
RS880D Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



DUAL X8 ENABLE < DUAL X8_ENABLE 24





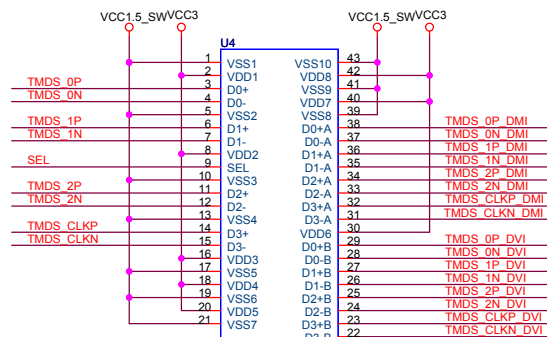
Elitegroup Computer Systems

File: **PCIEX16 SLOT & PCIe8 SLOT**

Size: Document Number **A890GXM-A** Rev **1.0**

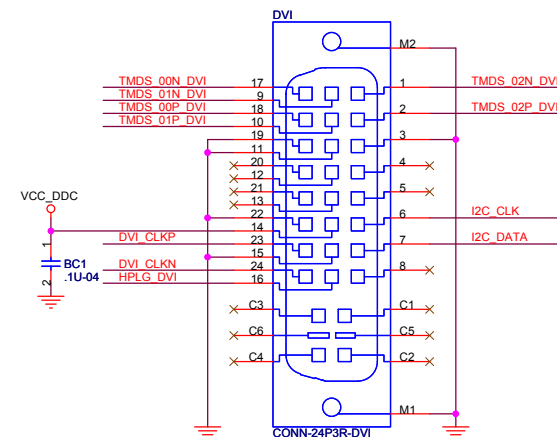
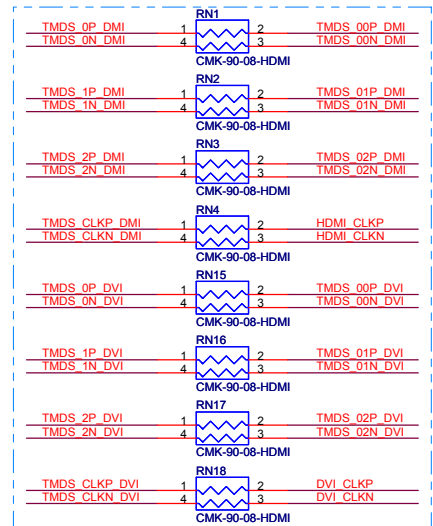
Date: Thursday, January 14, 2010 Sheet 19 of 38

17	HPLG	« HPLG
17	I2C_CLK	» I2C_CLK
17	I2C_DATA	» I2C_DATA
17	TMDS_0P	» TMDS_0P
17	TMDS_0N	» TMDS_0N
17	TMDS_1P	» TMDS_1P
17	TMDS_1N	» TMDS_1N
17	TMDS_2P	» TMDS_2P
17	TMDS_2N	» TMDS_2N
17	TMDS_CLKP	» TMDS_CLKP
17	TMDS_CLKN	» TMDS_CLKN
15	GFX_C_TX0P	GFX_C_TX0P
15	GFX_C_TX0N	GFX_C_TX0N
15	GFX_C_TX1P	GFX_C_TX1P
15	GFX_C_TX1N	GFX_C_TX1N
15	GFX_C_TX2P	GFX_C_TX2P
15	GFX_C_TX2N	GFX_C_TX2N
15	GFX_C_TX3P	GFX_C_TX3P
15	GFX_C_TX3N	GFX_C_TX3N

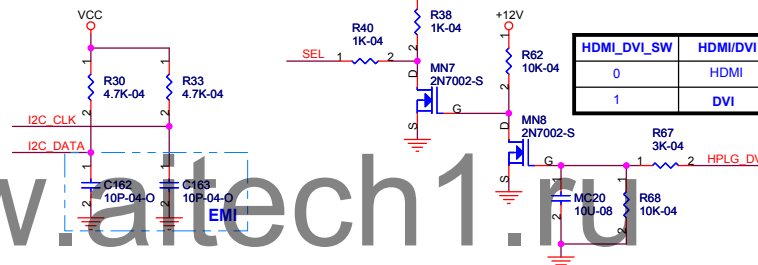
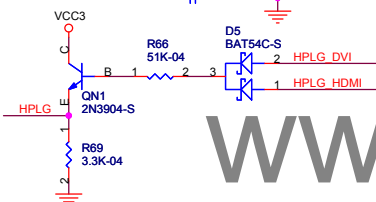
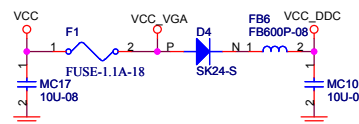
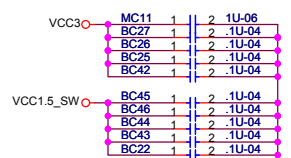


SEL	HDMI/DVI
0	HDMI
1	DVI

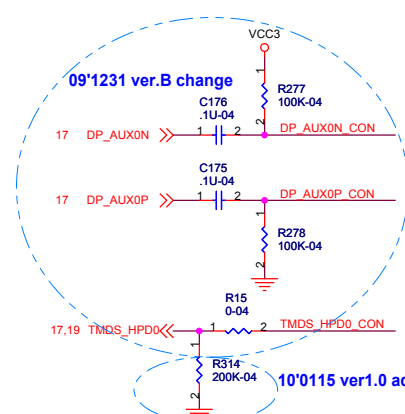
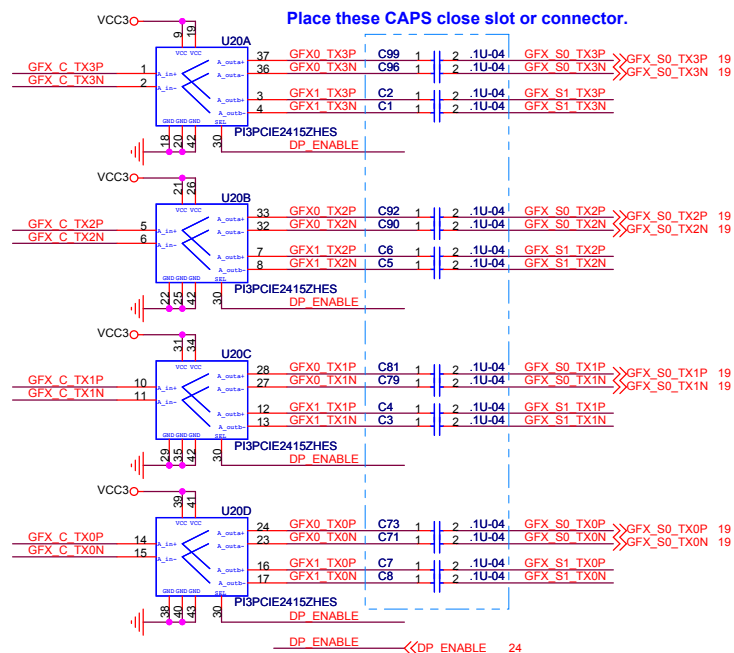
Change the PI3HDMI412FT-BZHES to
ASM1445:(02-342-445070),Because of
Leakage from the PI3HDMI412FT
output differential line.



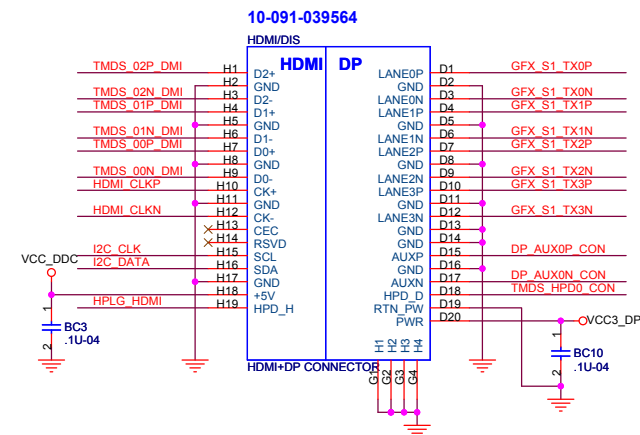
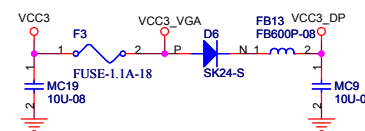
Vout=1.25V*(1+Rb/Rt)

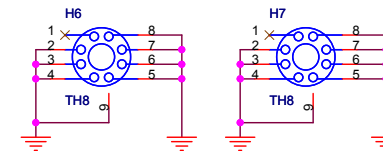
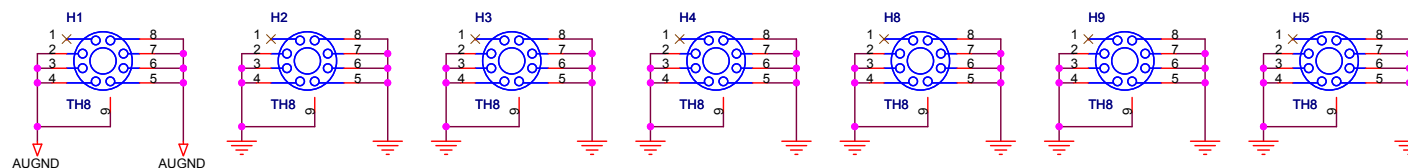
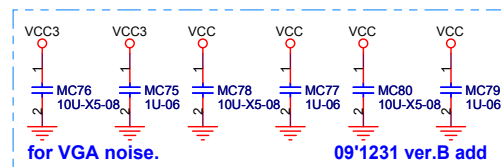
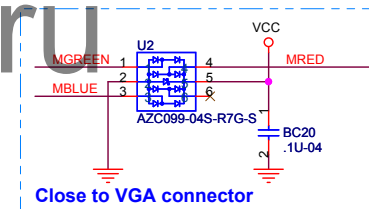
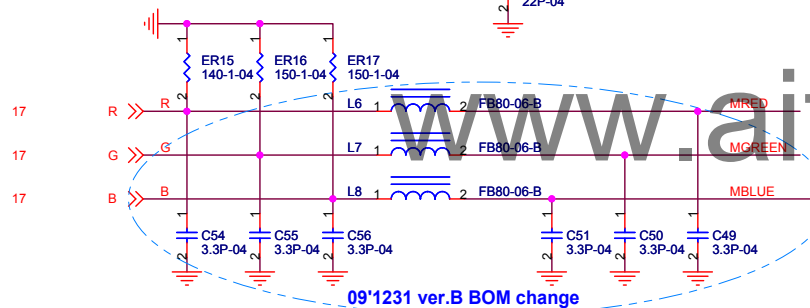
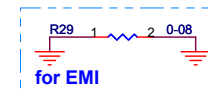
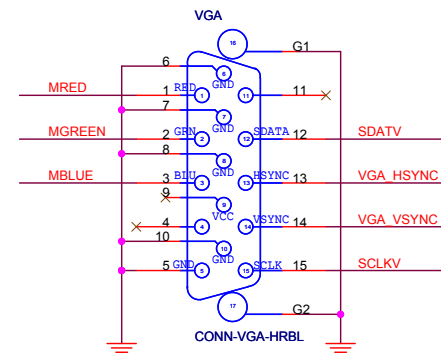
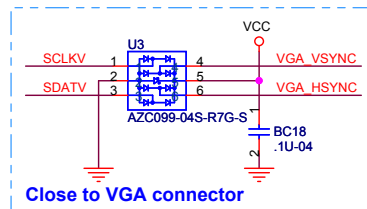
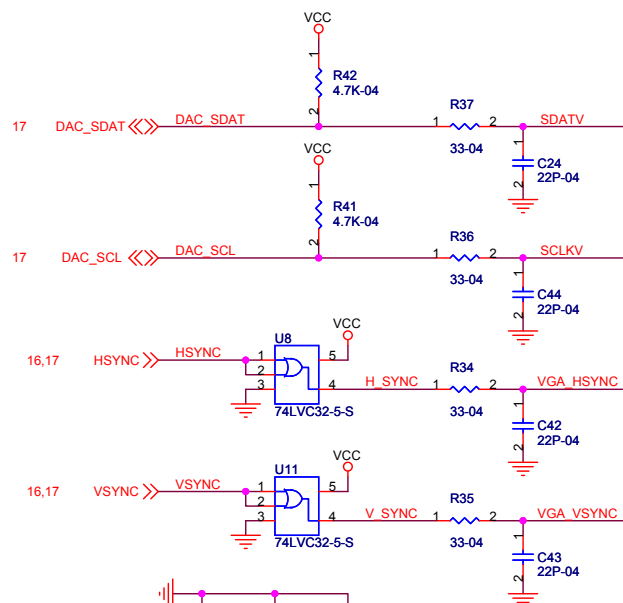


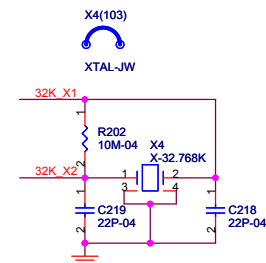
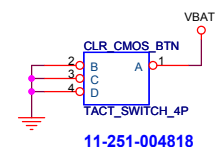
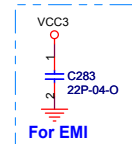
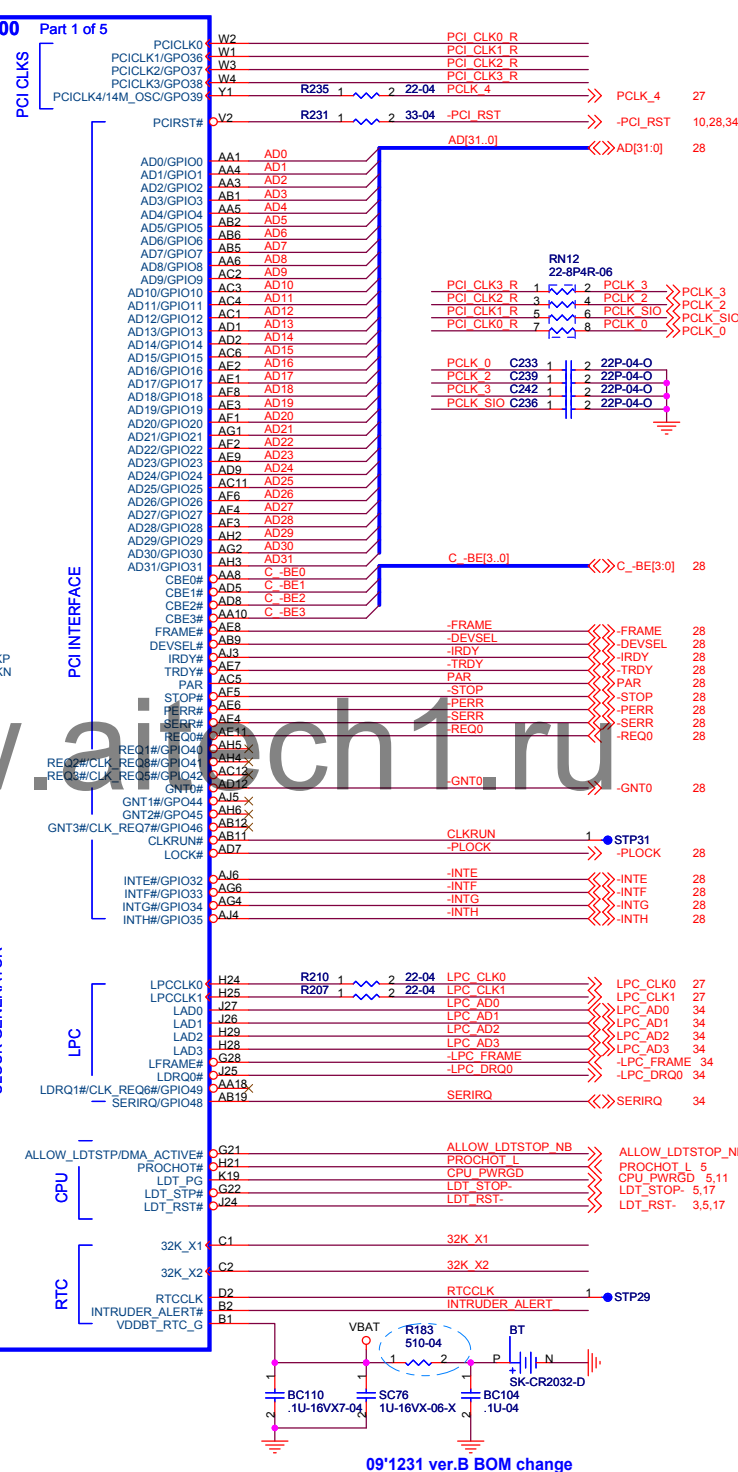
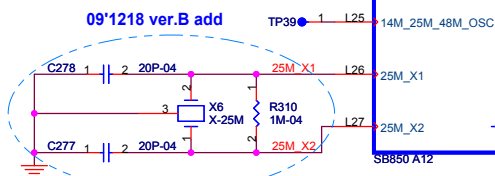
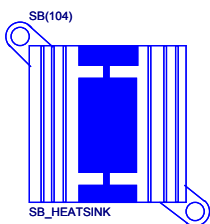
HDMI_DVI_SW	HDMI/DVI
0	HDMI
1	DVI

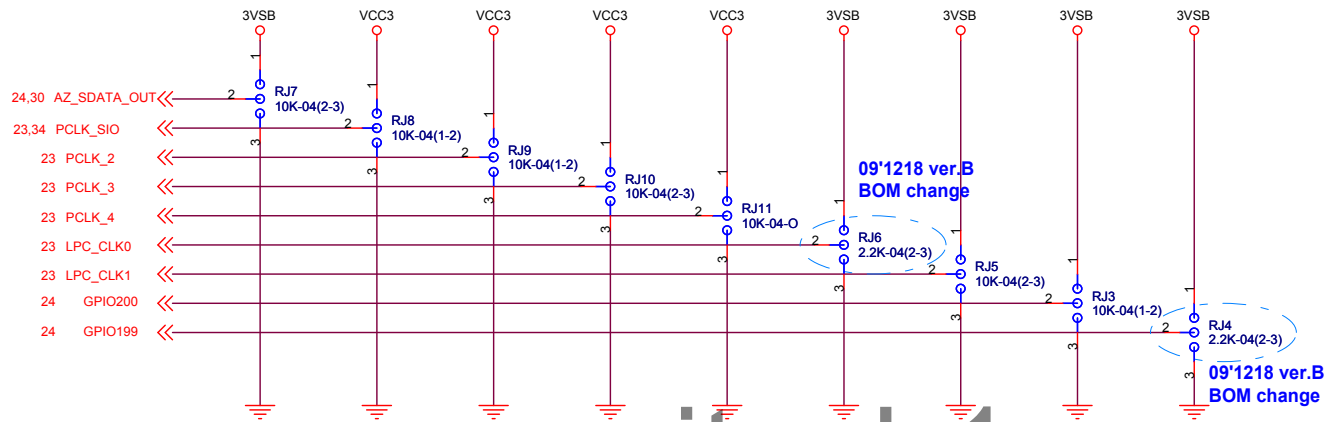


GFX_MODE_SELECT	GFX SLOTS MODE
0	PCIEX16 SLOT (DEFAULT)
1	DISPLAY PORT





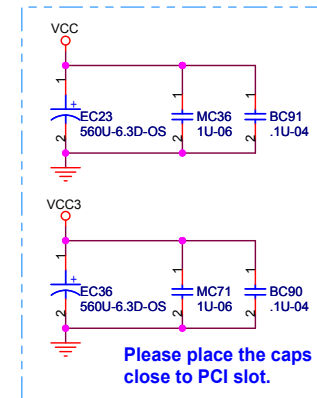
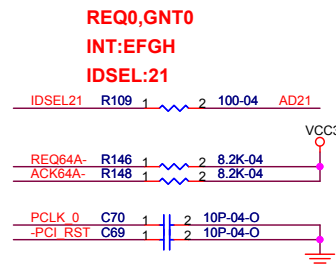
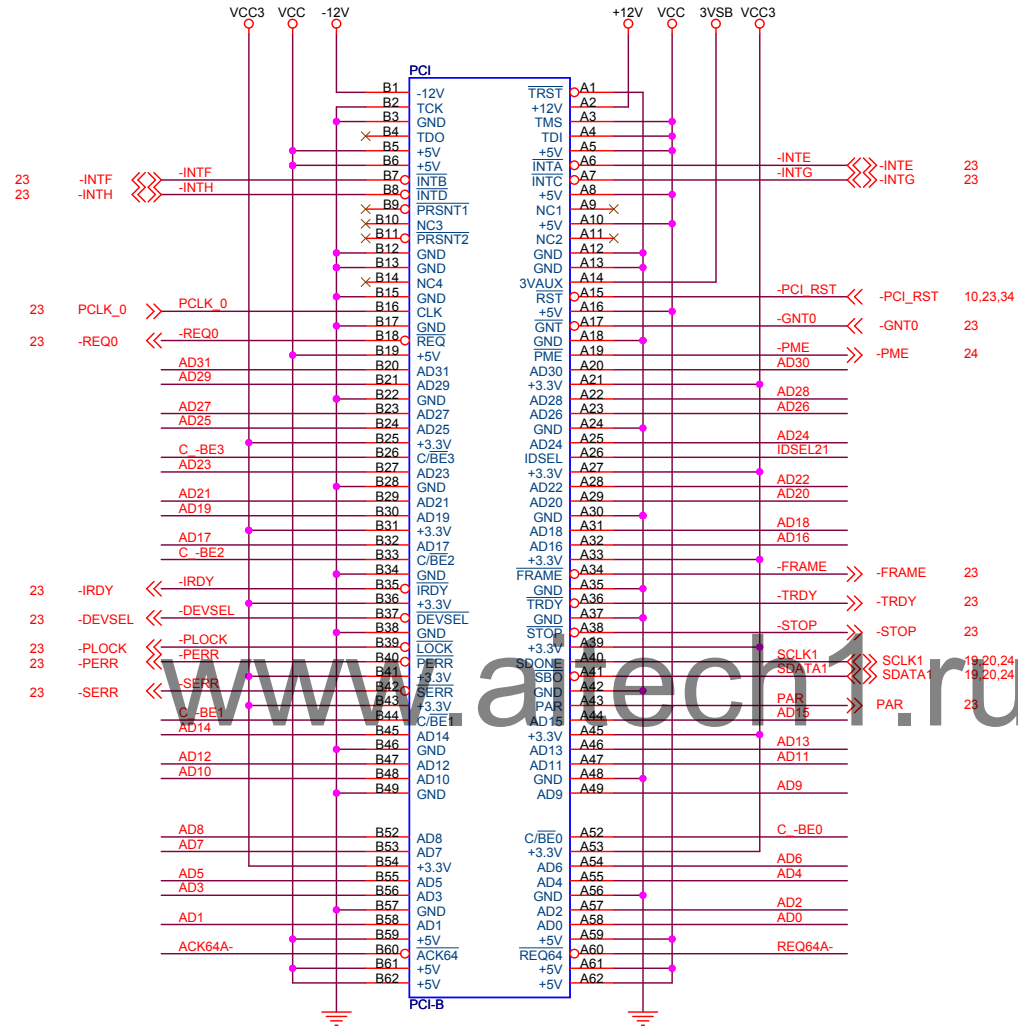




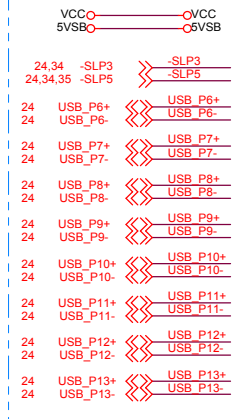
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GP200	GP199
PULL HIGH	LOW POWER MODE DEFAULT	ALLOW PCIE GEN2 DEFAULT	Watchdog Timer Enabled DEFAULT	USE DEBUG STRAP DEFAULT	Non Fusion CLOCK MODE	EC ENABLED DEFAULT	Internal CLOCK MODE	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	Reserved DEFAULT	FORCE PCIE GEN1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	External CLOCK MODE DEFAULT	L, H = LPC ROM L, L = FWH ROM	

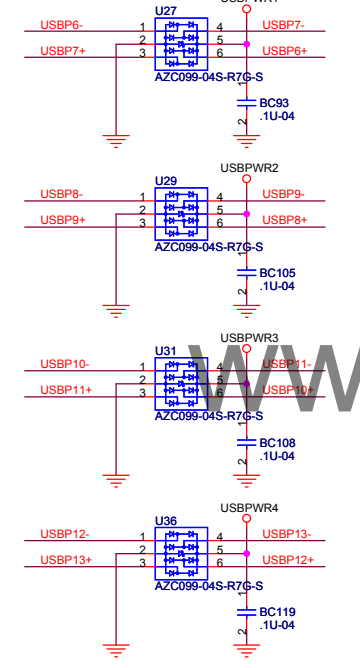
23 AD[31:0] <<> AD[31..0]
23 C_-BE[3:0] <<> C_-BE[3..0]



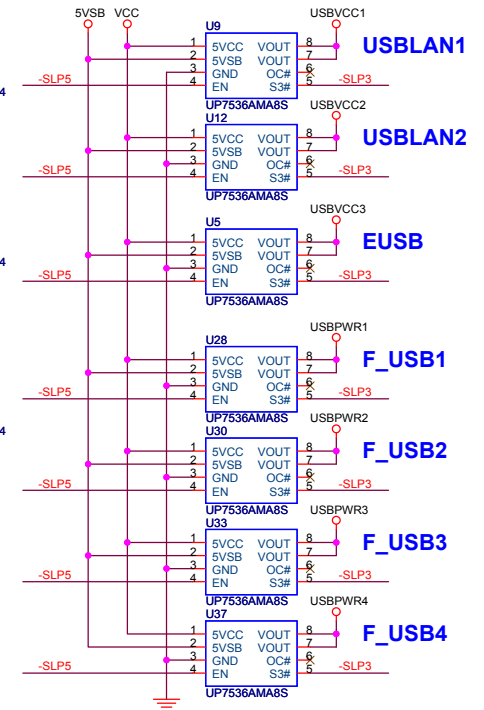
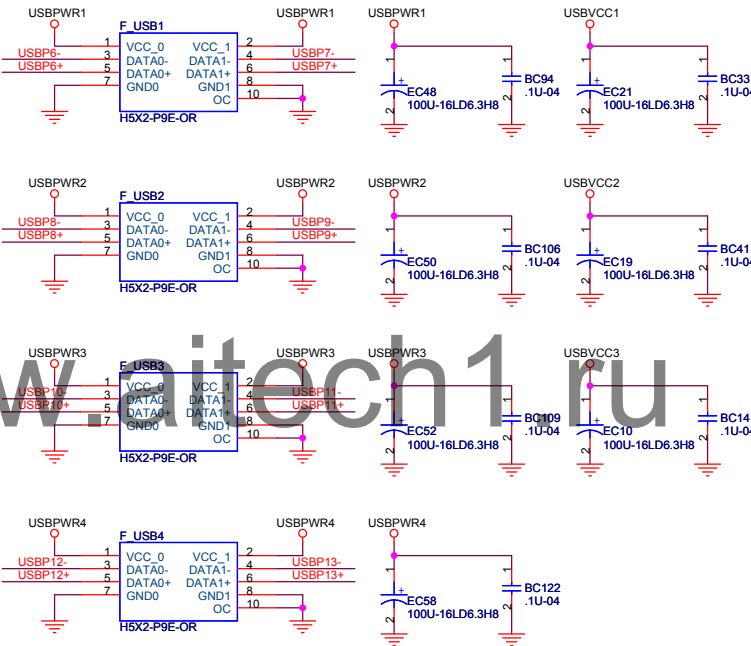
External Connection



Close to F_USB Header



FRONT SIDE USB HEADER



5VSB ○ ————— ○ 5VSB

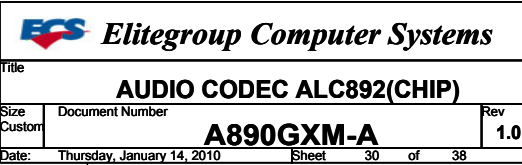
24 AZ_RST » AZ_RST

24 AZ_BIT_CLK » AZ_BIT_CLK

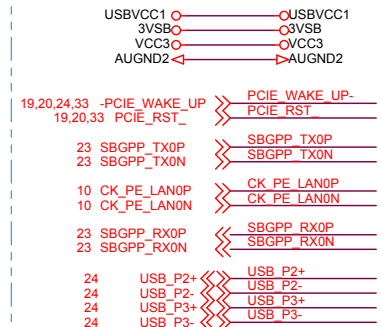
24 AZ_SYNC » AZ_SYNC

24 AZ_SDATA_IN » AZ_SDATA_IN

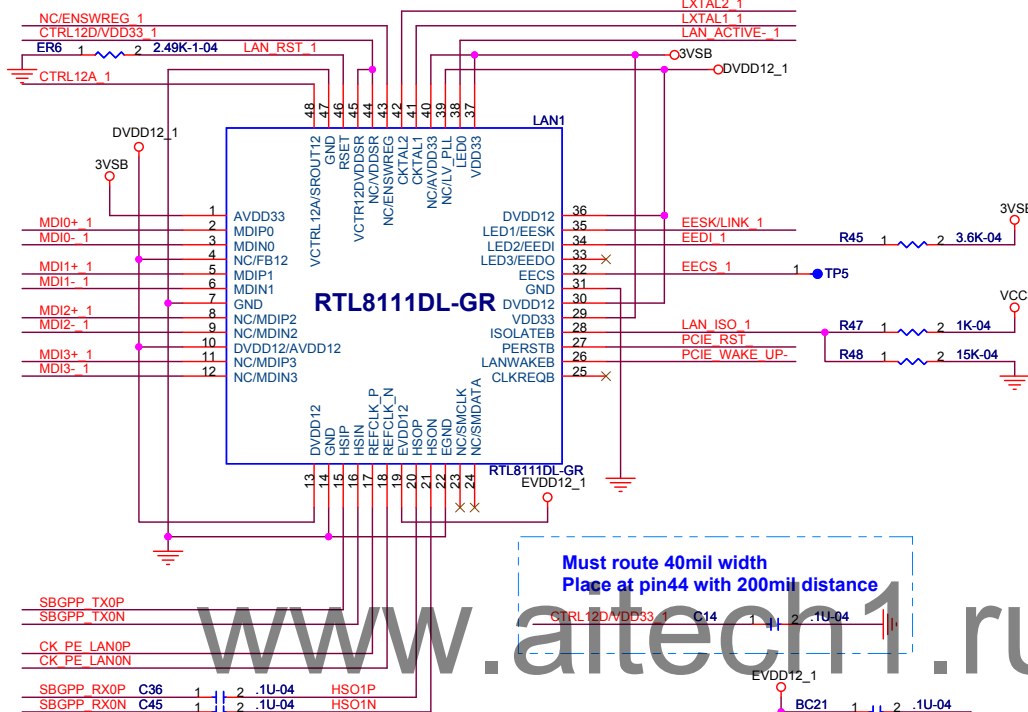
24,27 AZ_SDATA_OUT << AZ_SDATA_OUT



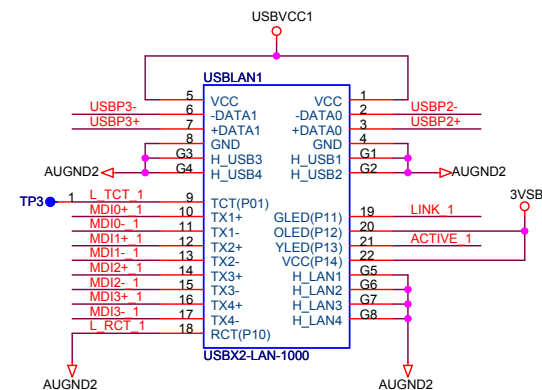
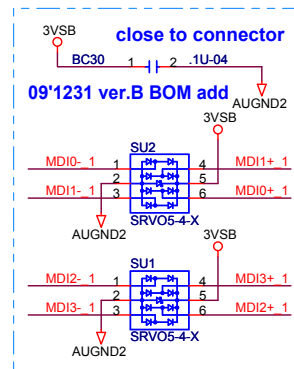
External Connection



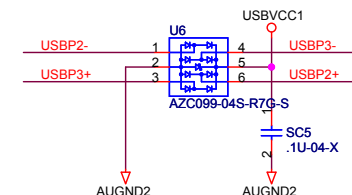
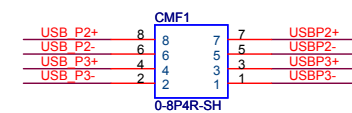
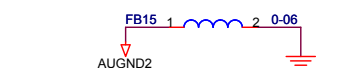
RSET電阻需close to LAN
Trace need GND shielding



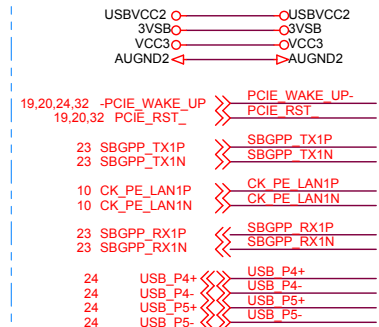
Must route 40mil width
Place at pin44 with 200mil distance



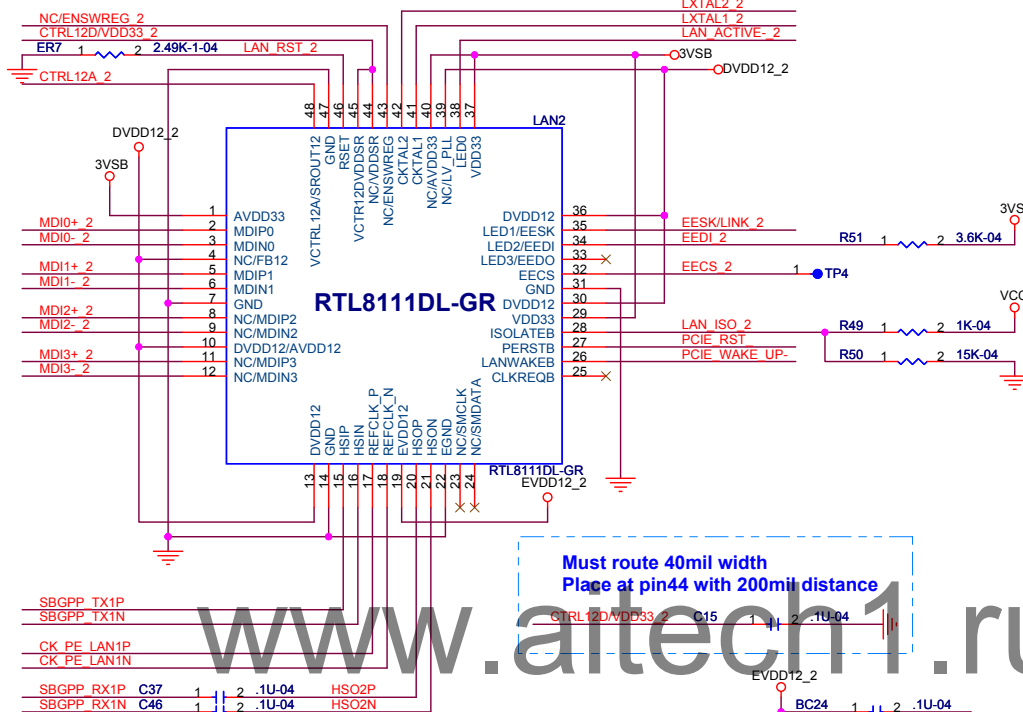
Link: Green on
Active: Yellow blinking



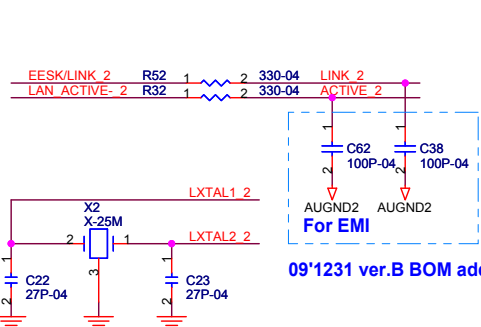
External Connection



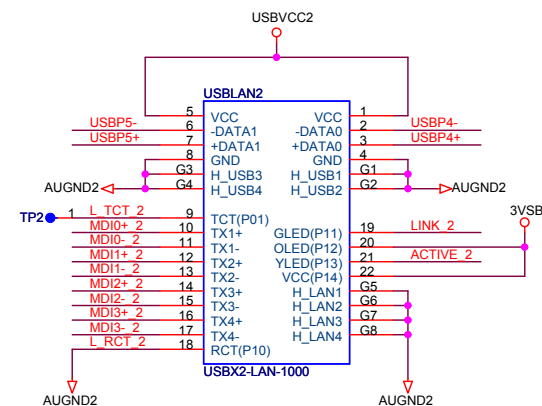
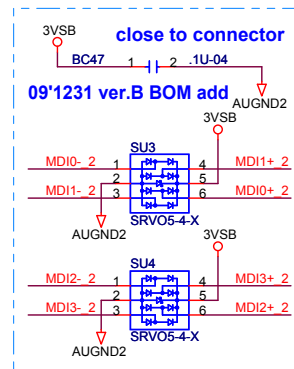
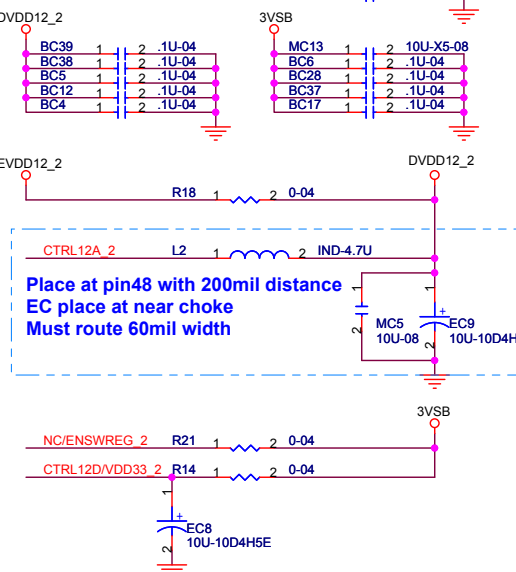
RSET电阻需close to LAN
Trace need GND shielding



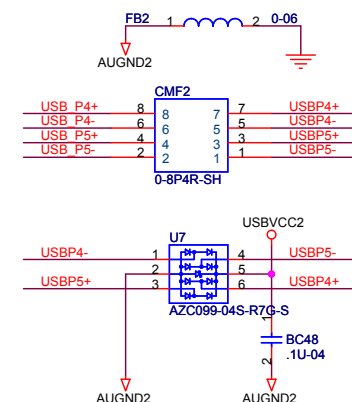
Must route 40mil width
Place at pin44 with 200mil distance



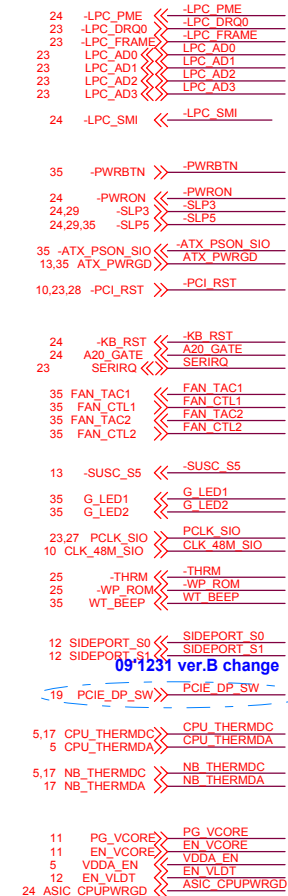
09'1231 ver.B BOM add



Link: Green on
Active: Yellow blinking



External Connection



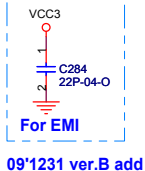
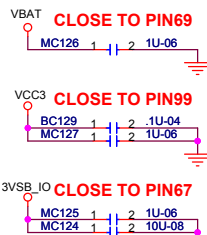
09'1231 ver.B change

09'1231 ver.B change

09'1231 ver.B change

HW STRAPPING

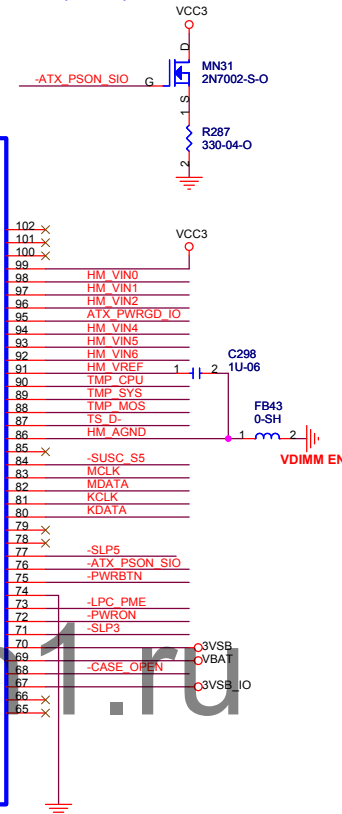
JP1 Pin 36	Flashseg1_EN	h	Disabled.
JP3 Pin 124	CHIP_SEL	h	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	KB_PWR_EN	h	Chip selection in Configuration
JP3 Pin 124	FAN_CTL_SEL	h	K8 power sequence function is disabled
JP5 Pin 46	WDT_EN	h	The default value of EC Index 15h/16h/17h is 00h
JP5 Pin 46	WDT_EN	h	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin 46	WDT_EN	h	The default value of EC Index 15h/16h/17h is 7Fh
JP5 Pin 46	WDT_EN	h	Disable WDT to rest PWROK
JP5 Pin 46	WDT_EN	h	Enable WDT to rest PWROK



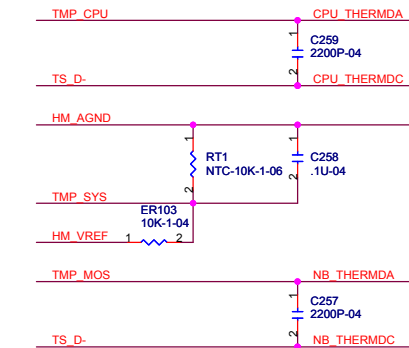
01-230-721091

IT8721F BX

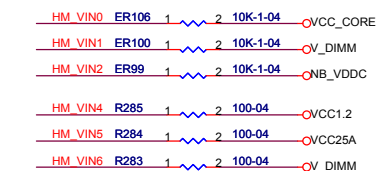
Pin99(AVCC3) Bleed-OFF circuit



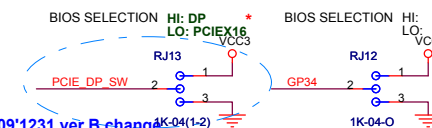
Thermal Monitor



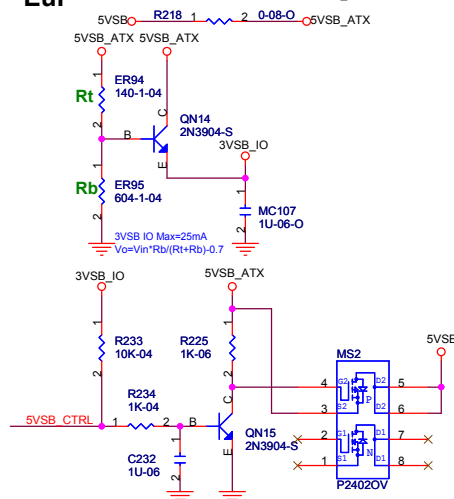
Voltage detection & AMD K8 power sequence

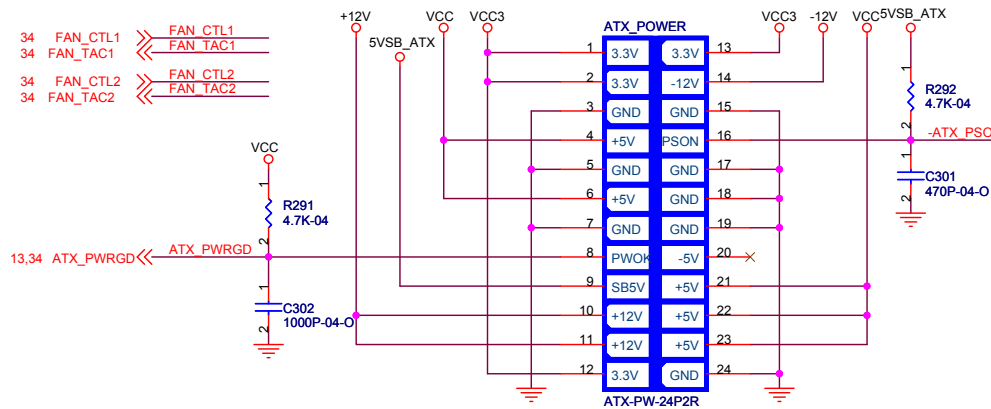


BIOS SELECTION

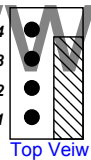
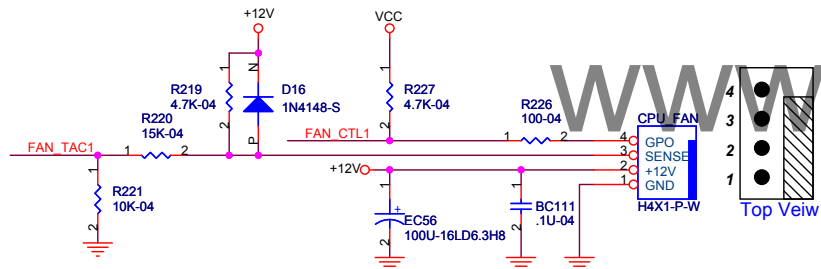
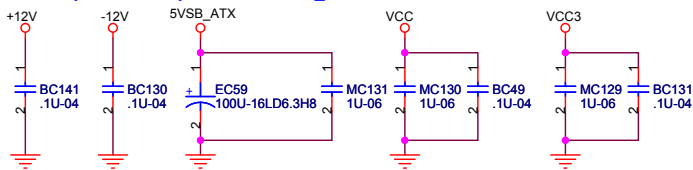


EuP

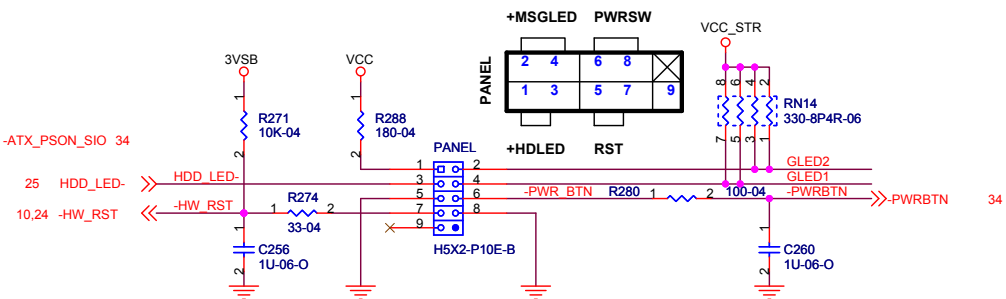
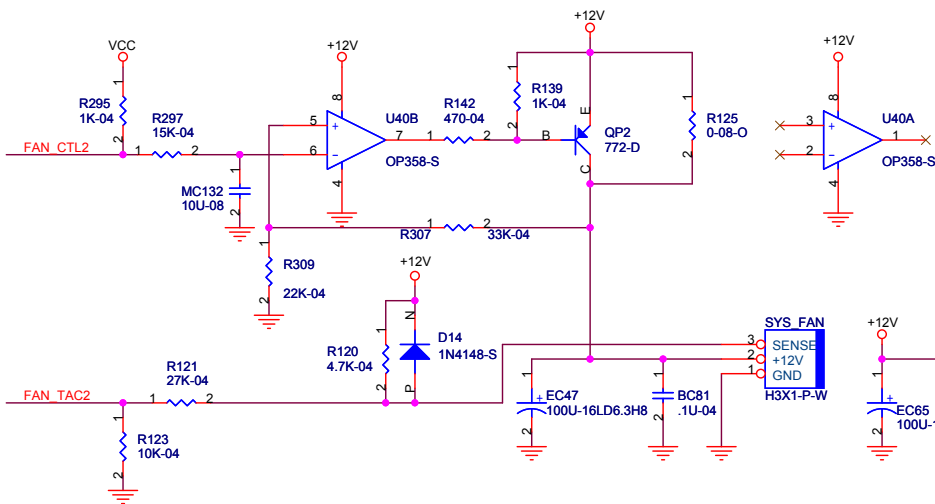




Please place the caps close to ATX_POWER connector.



Top Veiw



ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%

